BENHA UNIVERSITY
FACULTY OF ENGINEERING AT SHOUBRA

ECE-322

Electronic Circuits (B)

Lecture #11
Programming the Spartan-3E FPGA Board

Instructor:

Dr. Ahmad El-Banna

SPRING 2015

Agenda

- Why Spartan-3E ?
- Step by Step Example

Why Spartan-3E ?

- Simply, it is available in our lab ☺

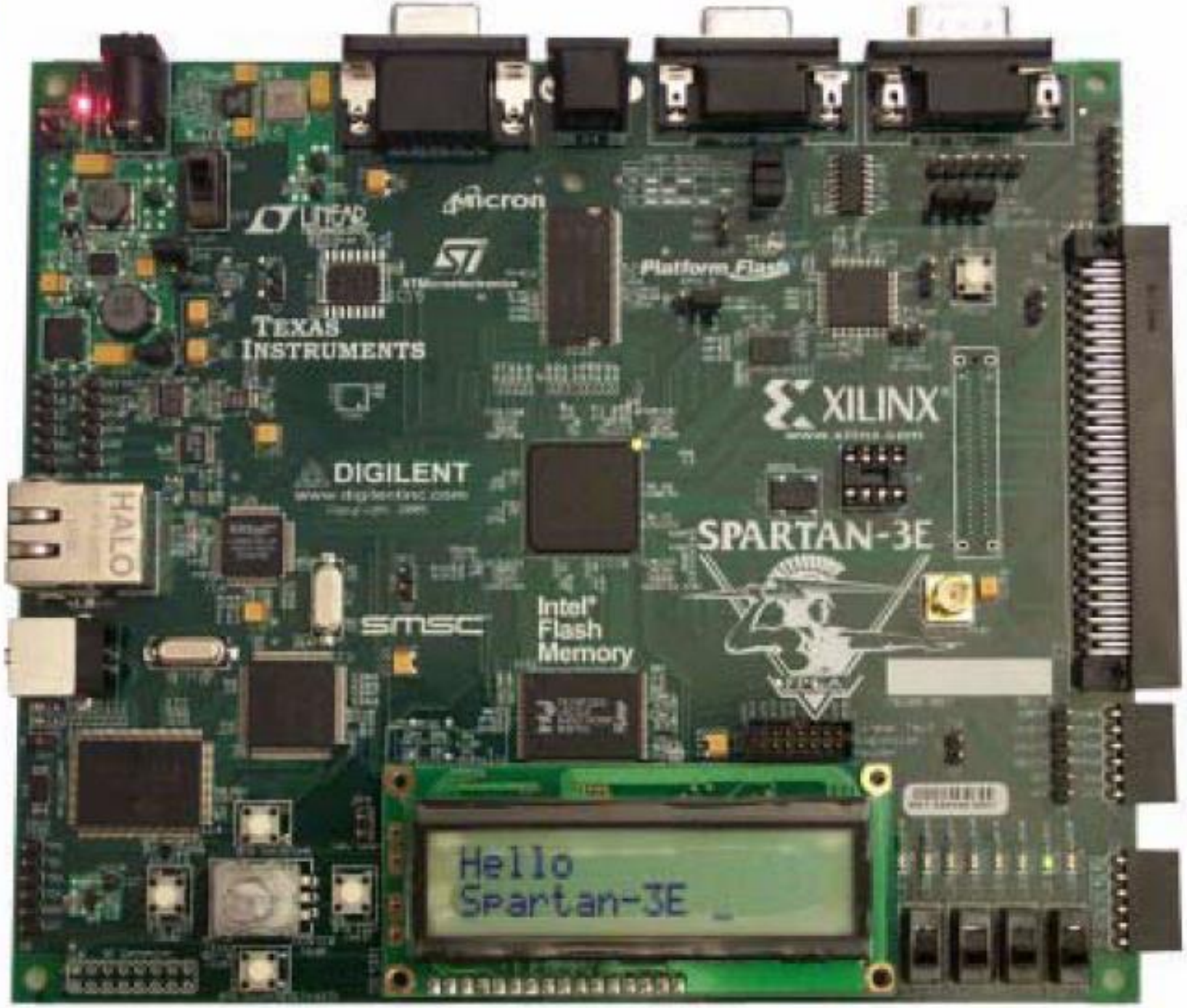
- Technically,
  - It's one of 5 platforms each delivering a unique cost-optimized balance of programmable logic, connectivity, and dedicated hard IP for your low-cost applications.
  - It is used for Logic Optimized applications.
  - For applications where logic densities matter more than I/O count Ideal for logic integration, DSP co-processing and embedded control, requiring significant processing and narrow or few interfaces

Lecture Reference

- We will follow the presentation talks about:

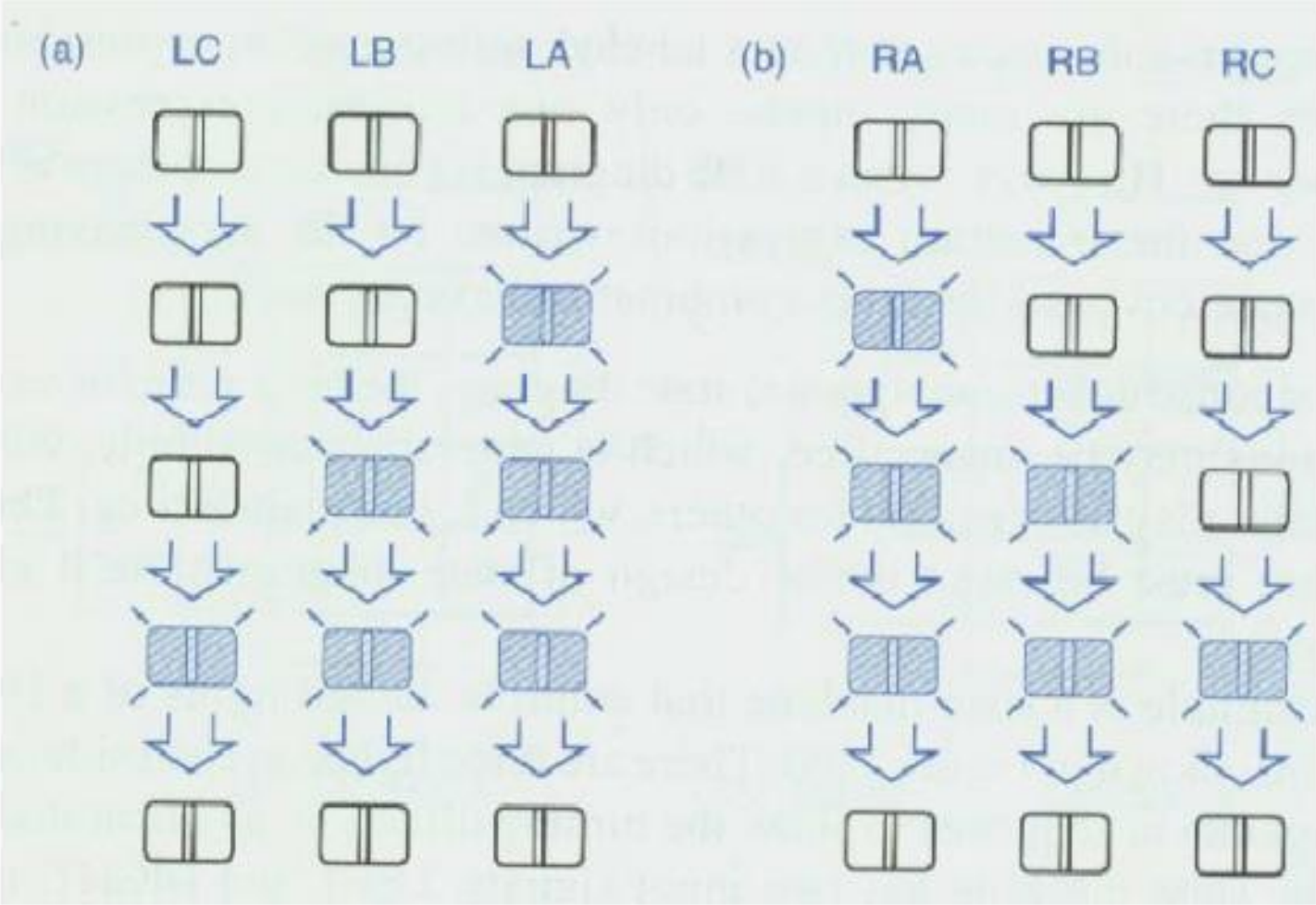
“How to program the FPGA SPARTAN-3E Board”

- By anonymous.
- Found at:
  - http://web.ewu.edu/groups/technology/Claudio/ee360/Protected/PresentationFPGA.pdf


Micron
Platform Flash
TEXAS INSTRUMENTS
XILINX
DIGILENT
SPARTAN-3E
smsc
Intel
Flash
Memory
Hello
Spartan-3E

The goal of the project is to write vhdl code to control the tail lights of a 1965 Ford Thunderbird and

then load this code into Spartan-3E FPGA Xilinx Board.



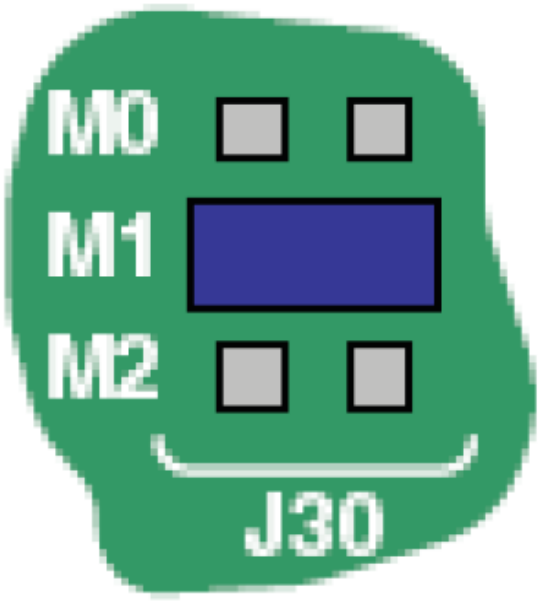
FPGA

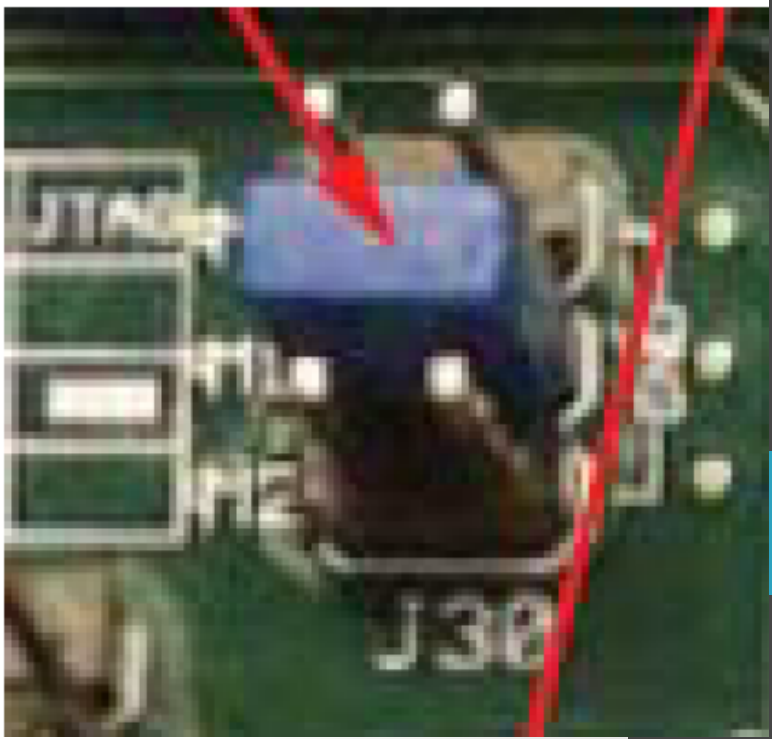
- To have a project ready to program the Spartan 3E FPGA, it was necessary to take a few preliminary steps. First, a project needed to be created in Xilinx. The project was named tail_light.
- the board has a 50MHz oscillator (see reference manual); therefore, the clock signal is so fast that the human eye is unable to see the sequence of the flashing lights. As a result, we had to add an additional file called counter.vhd, which will slow the incoming clock down.

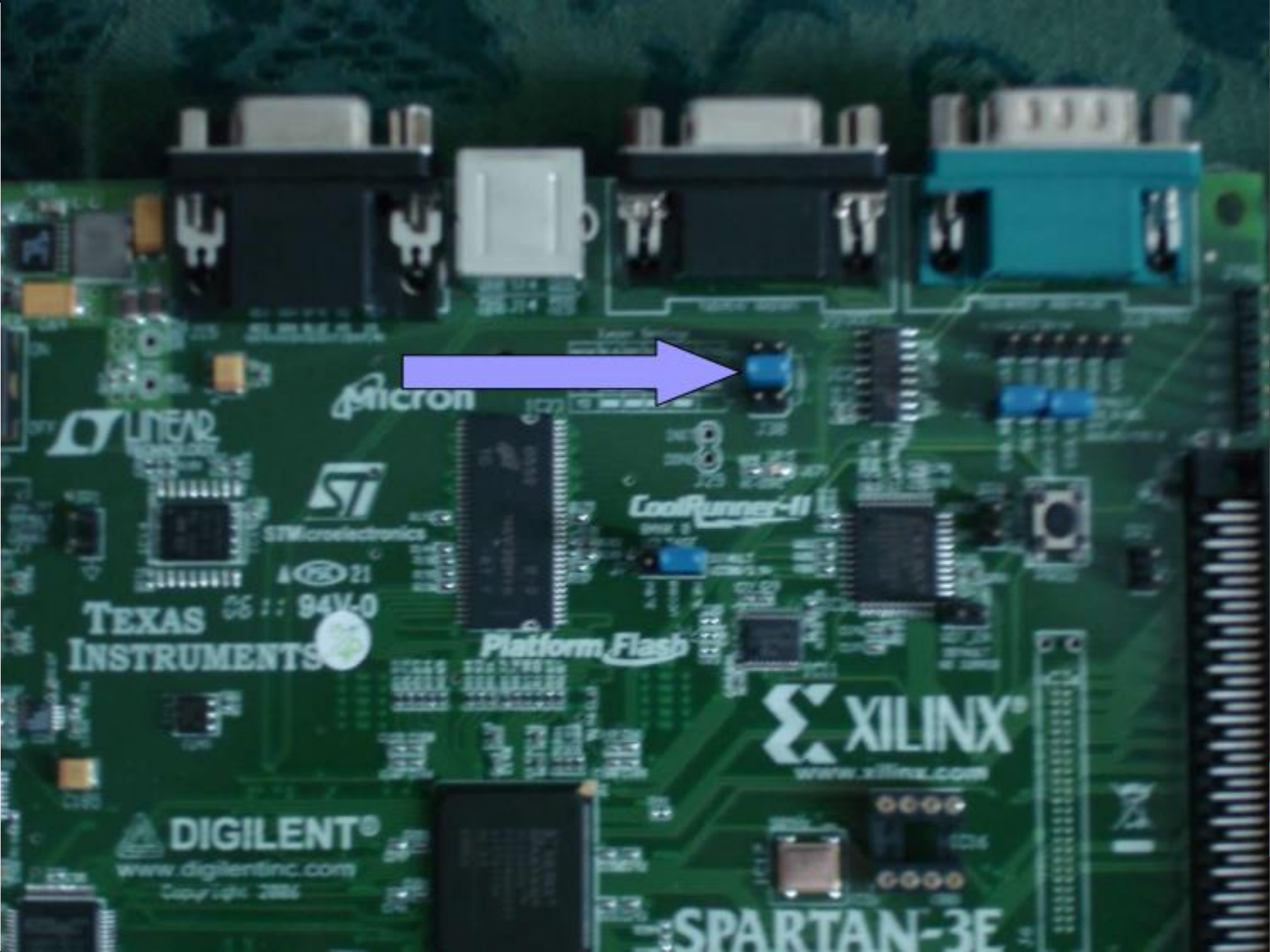
- In order for these two files to work together, we had to write the top_level.vhd file

Spartan-3E Configuration Mode Jumper Settings

- **Configuration Mode** - JTAG
- Download from host via USB JTAG port

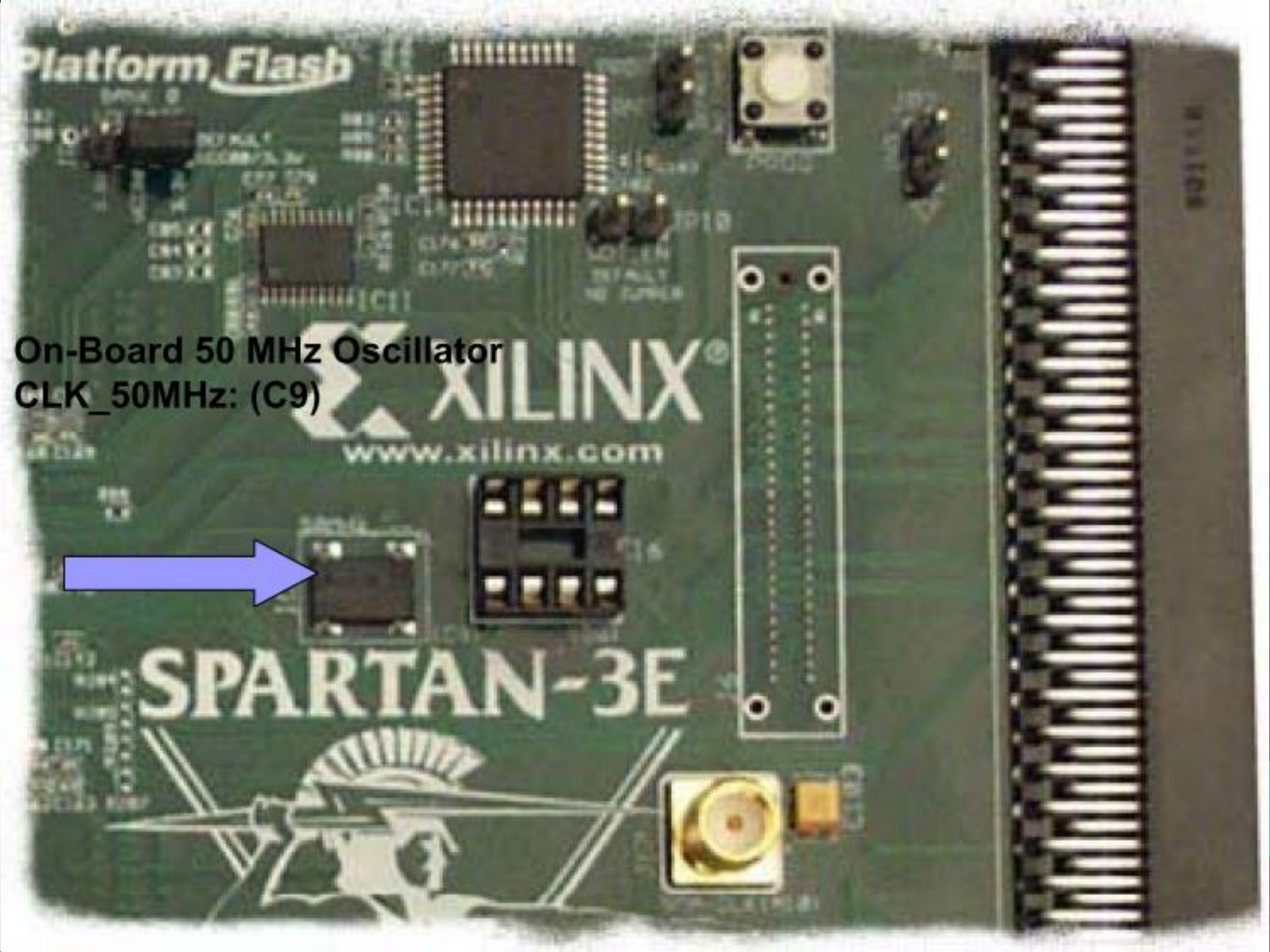




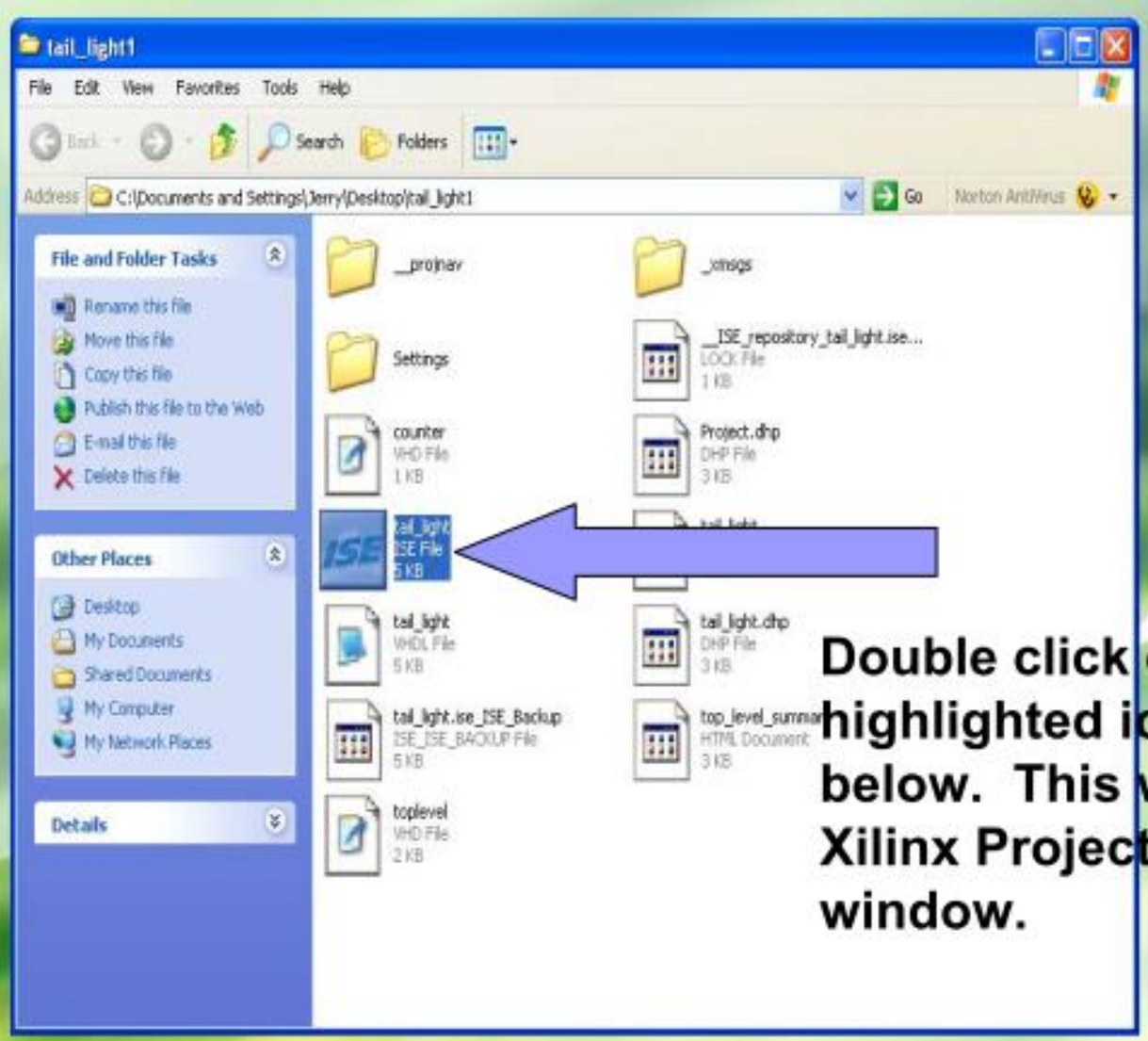

Micron
LINEAR TECHNOLOGY
STMicroelectronics
CoolRunner-II
Platform Flash
TEXAS INSTRUMENTS
XILINX
www.xilinx.com
DIGILENT
www.digilentinc.com
SPARTAN-3E

FPGA CLOCK INPUTS

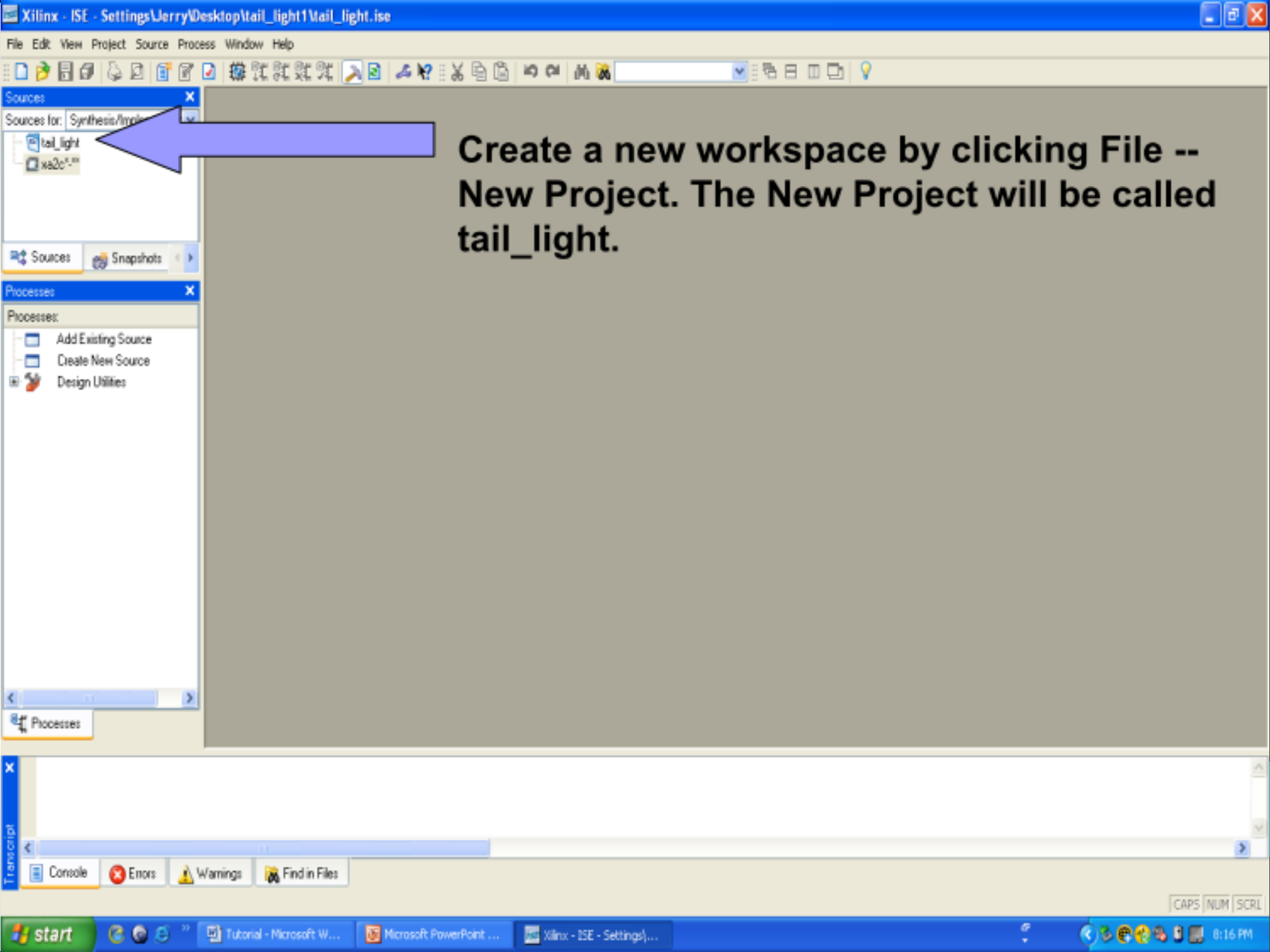
- **Clock Input FPGA Pin Global Buffer Associated DCM**
- CLK_50MHZ **C9** GCLK10 DCM_X0Y1
- CLK_AUX B8 GCLK8 DCM_X0Y1
- CLK_SMA A10 GCLK7 DCM_X1Y1

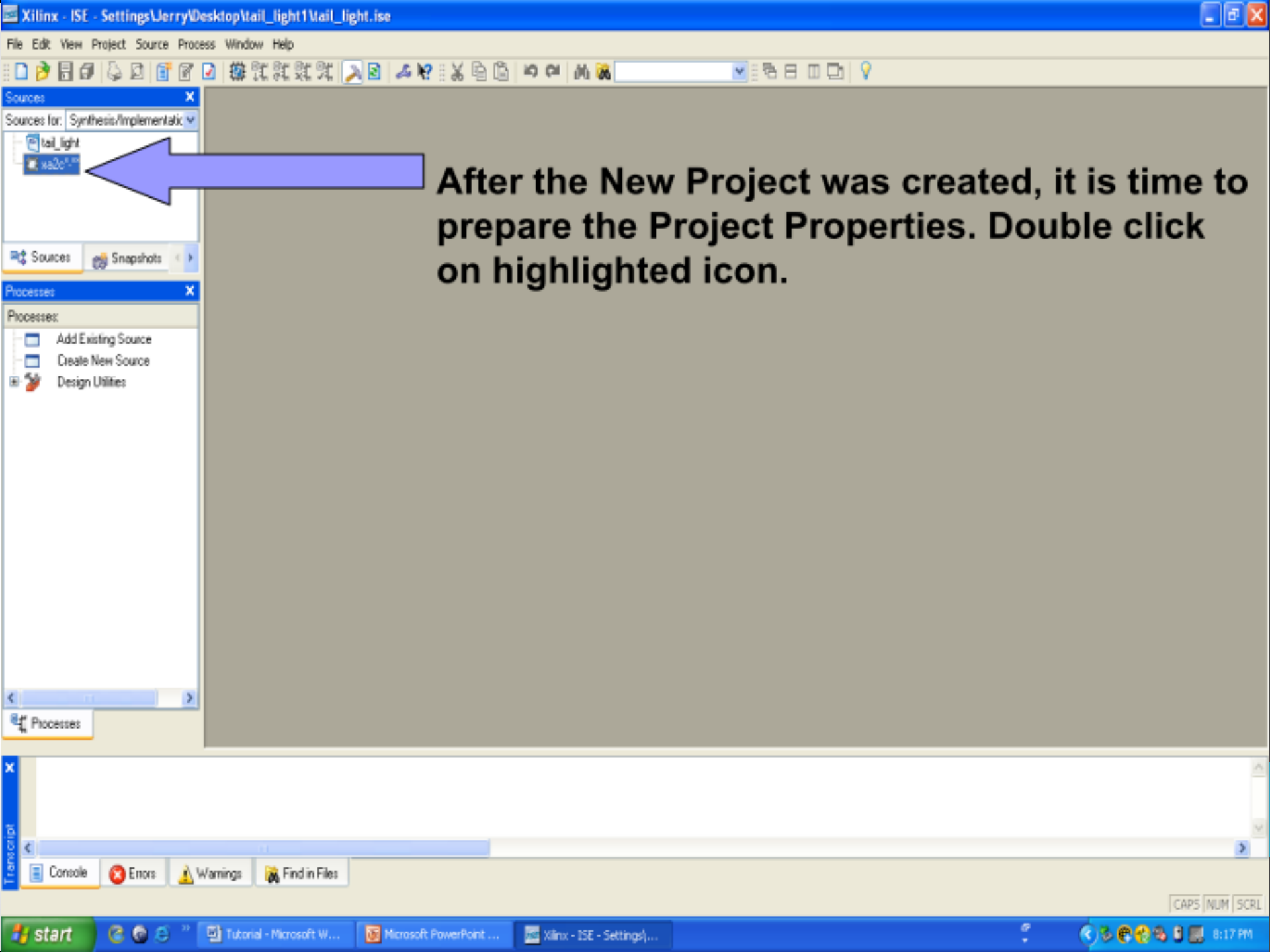


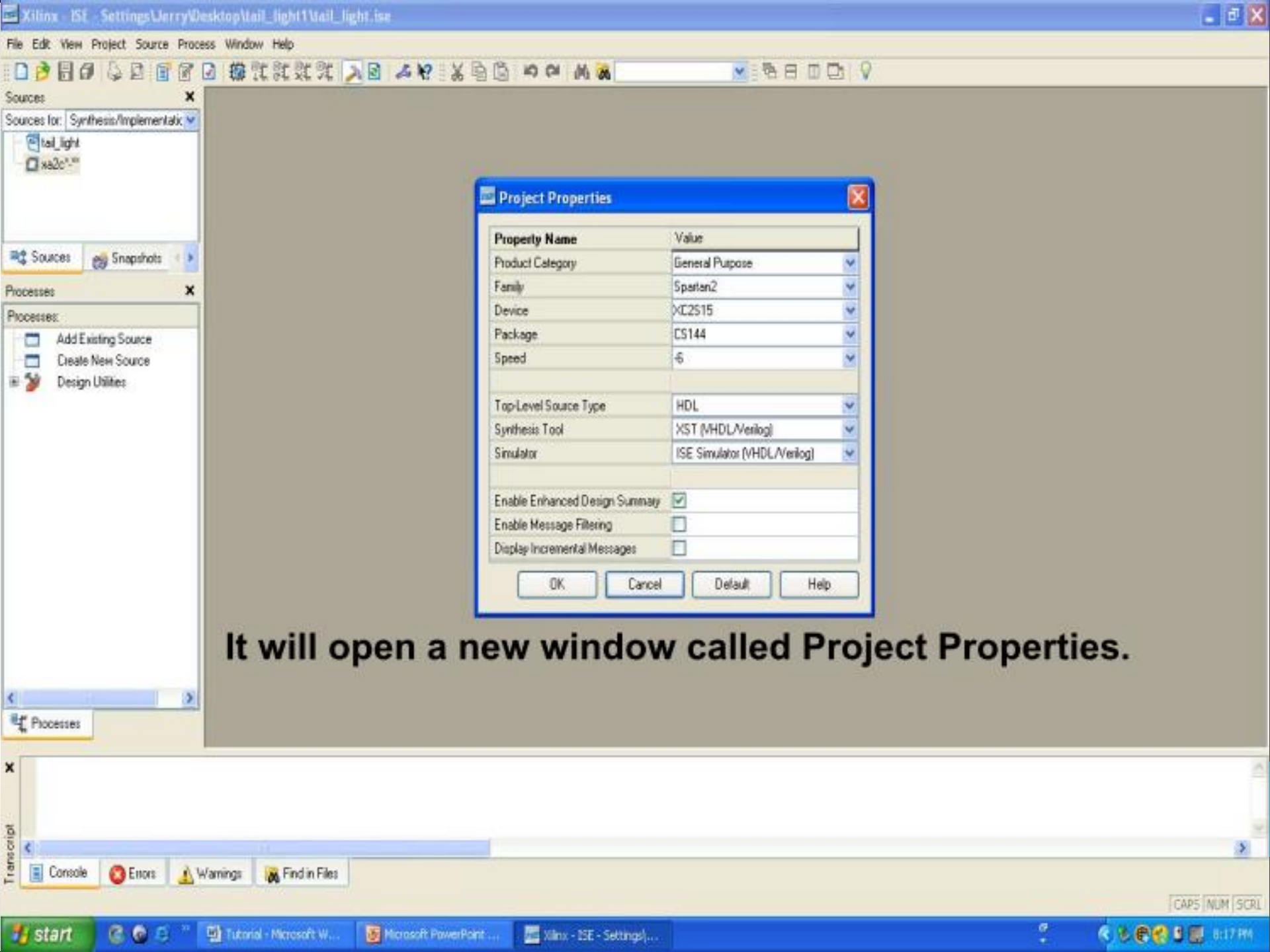
On-Board 50 MHz Oscillator
CLK_50MHz: (C9)

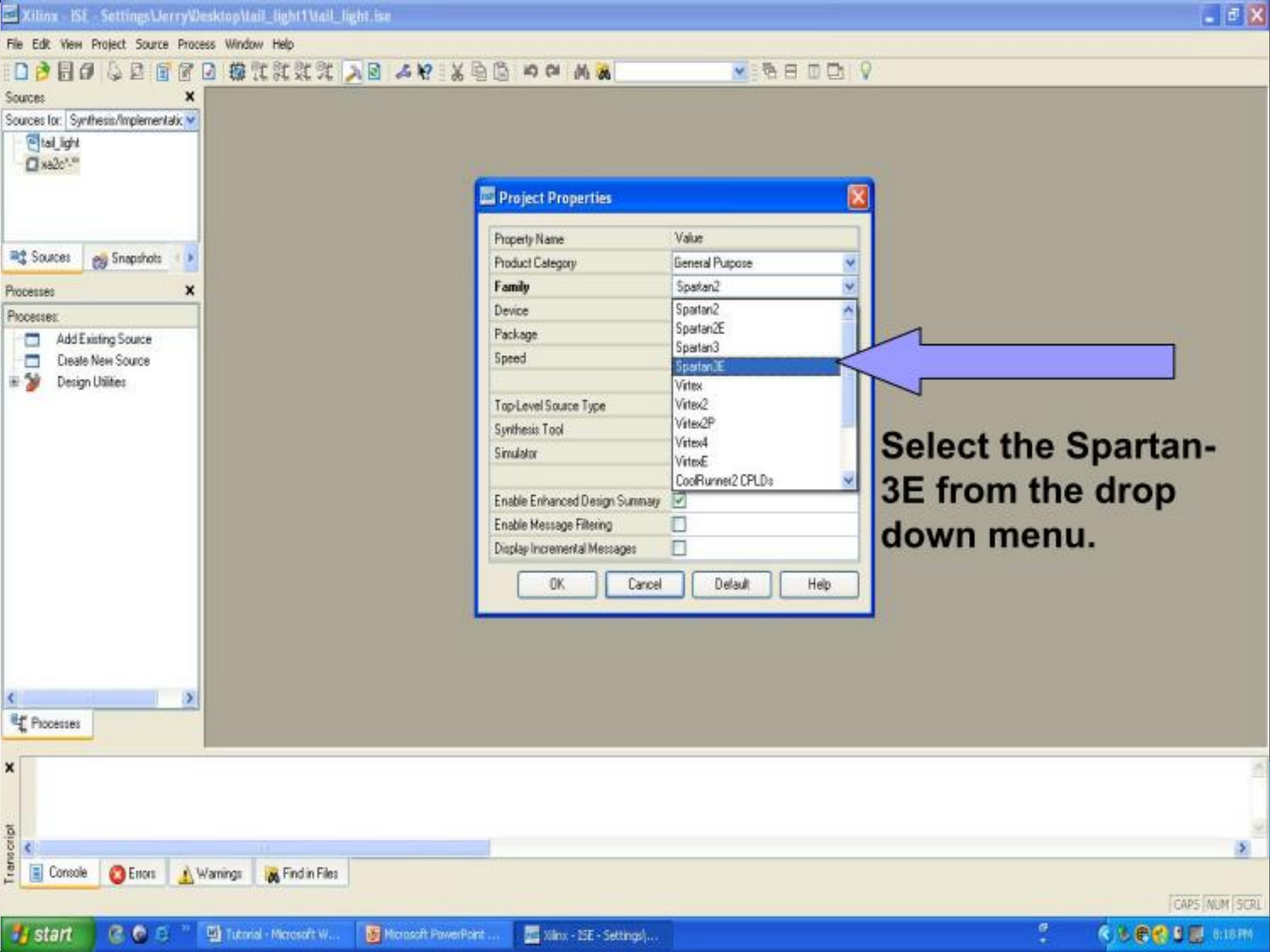


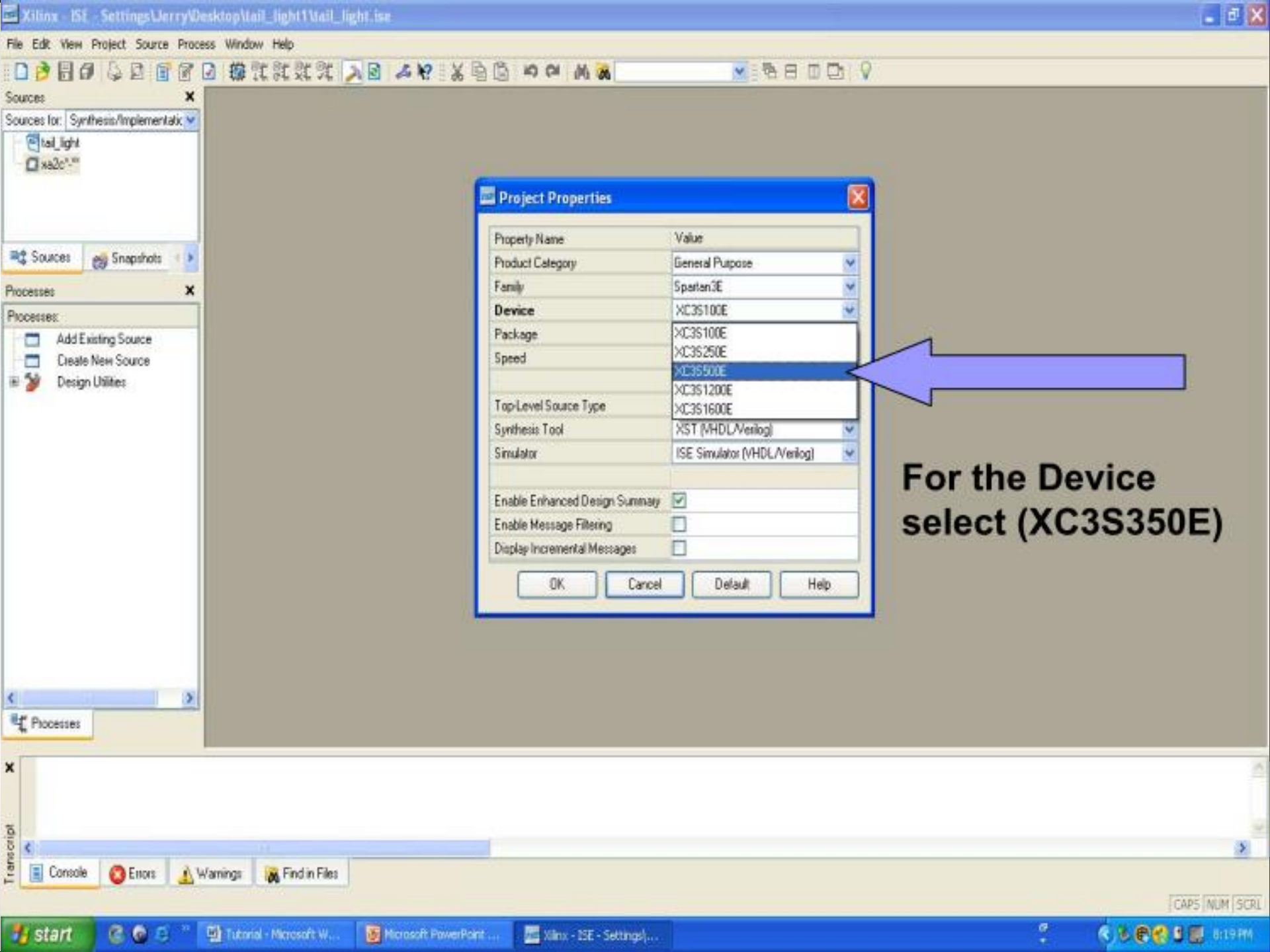
Double click on the highlighted icon shown below. This will open the Xilinx Project Navigator window.

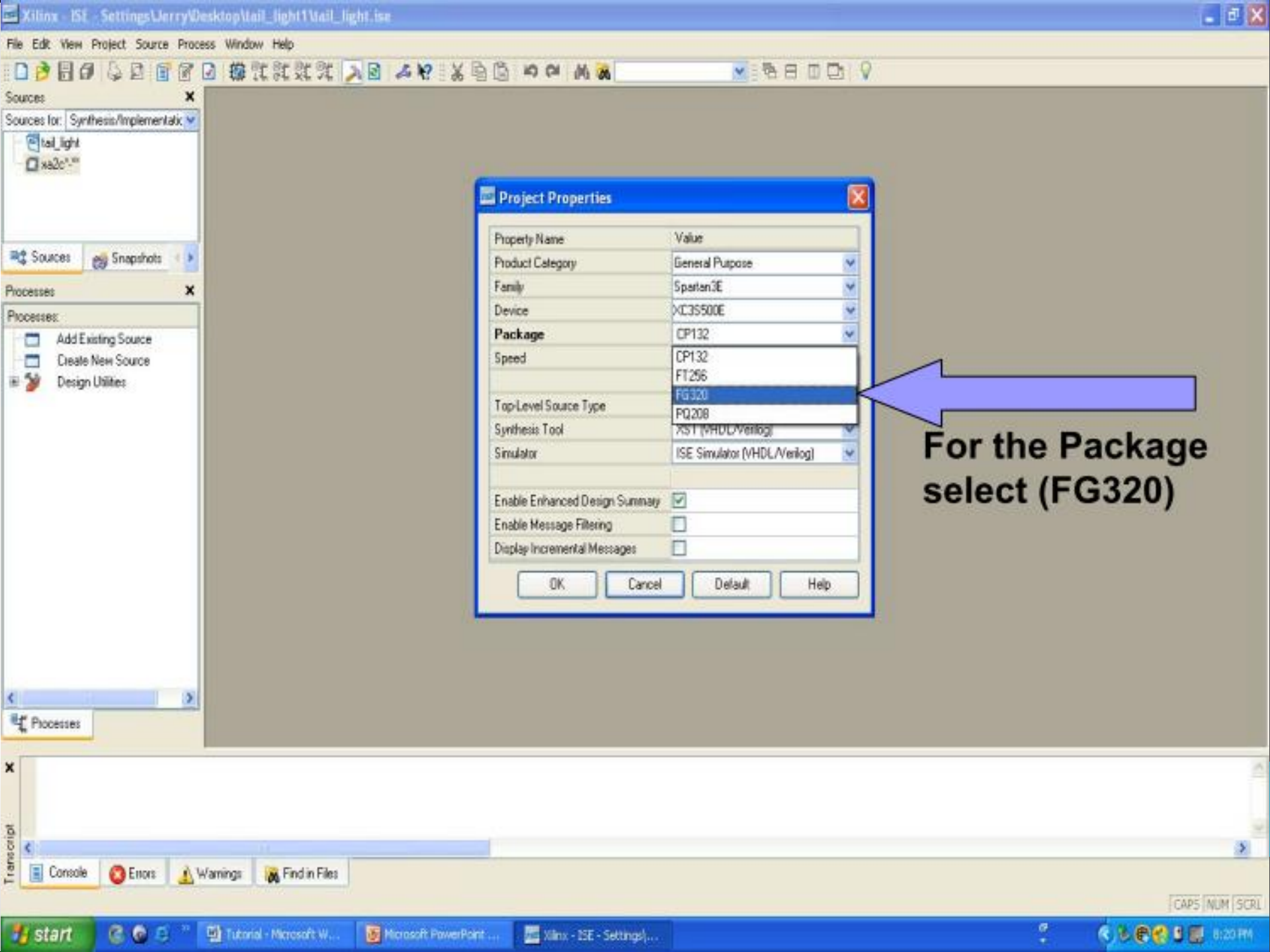

Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise
File Edit View Project Source Process Window Help
Sources
Sources for:
tail_light
Sources
Snapshots
Processes
Processes:
Add Existing Source
Create New Source
Design Utilities
Processes
Create a new workspace by clicking File -- New Project. The New Project will be called tail_light.
Transcript
Console
Errors
Warnings
Find in Files
CAPS NUM SCRL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
8:16 PM

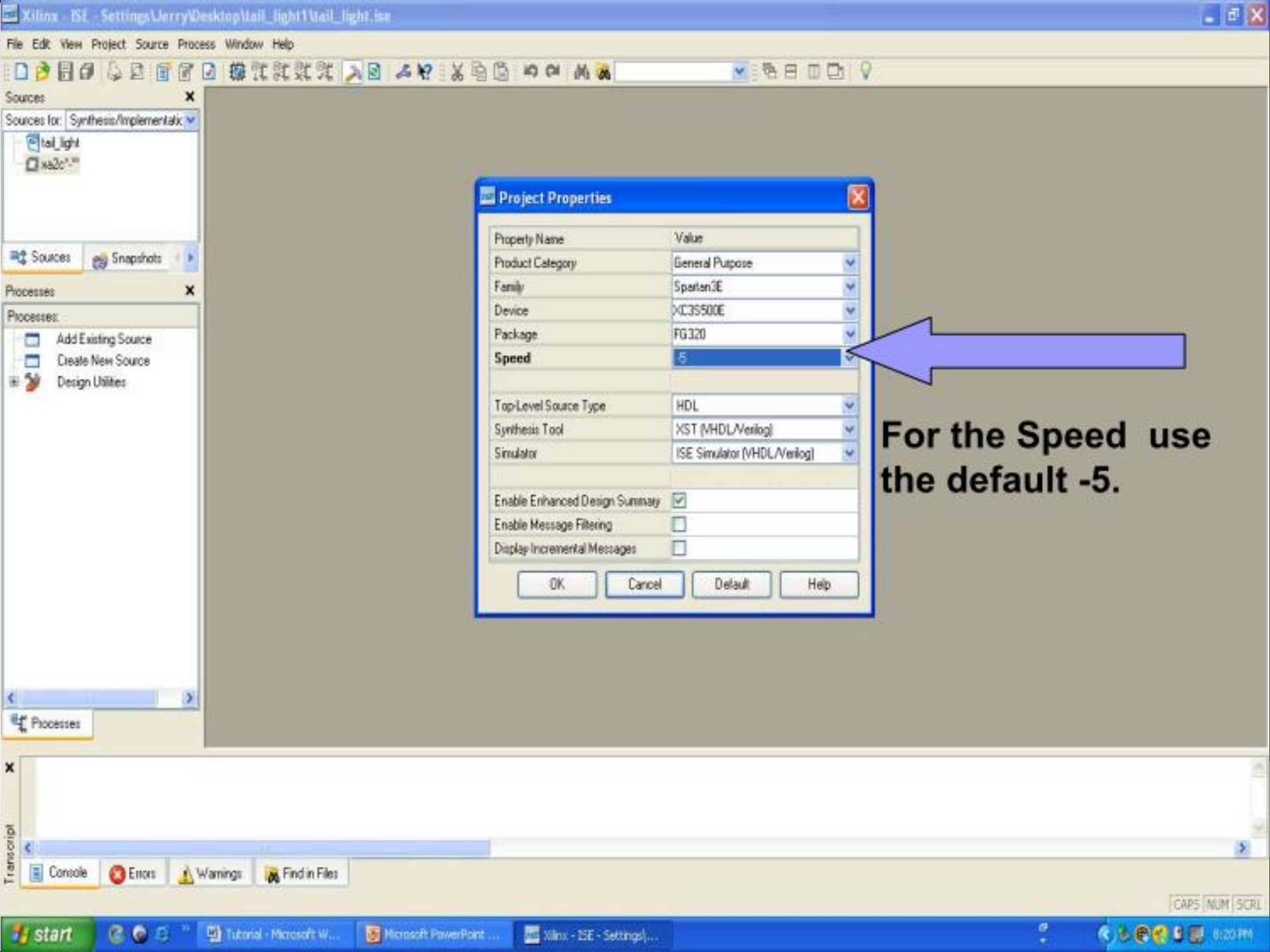

Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementatic
tail_light
Sources
Snapshots
Processes
Processes:
Add Existing Source
Create New Source
Design Utilities
Processes
After the New Project was created, it is time to prepare the Project Properties. Double click on highlighted icon.
Transcript
Console
Errors
Warnings
Find in Files
CAPS
NUM
SCRL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
8:17 PM

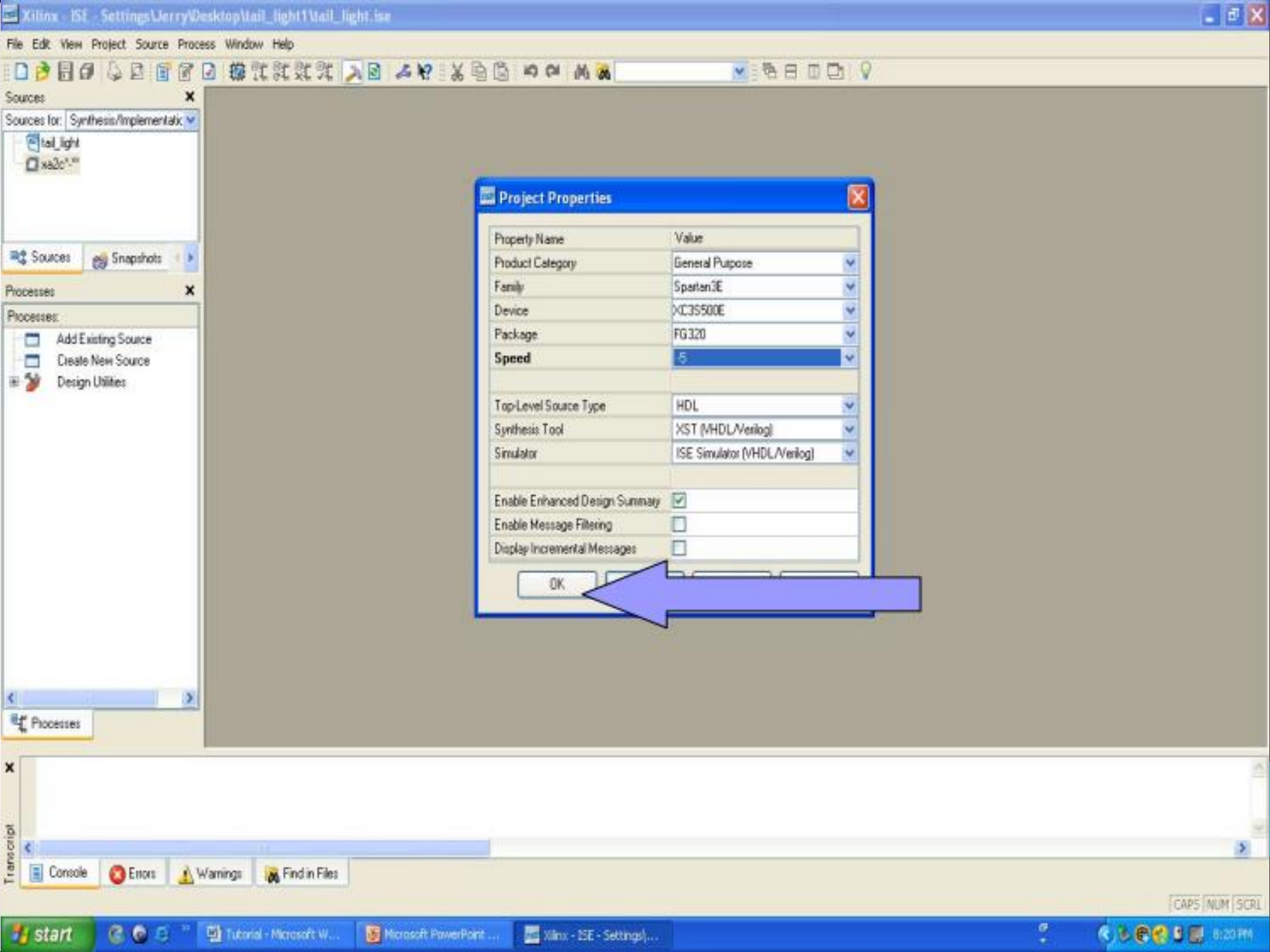

Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementation
tail_light
Sources
Snapshots
Processes
Processes:
Add Existing Source
Create New Source
Design Utilities
Processes
Project Properties
Property Name
Value
Product Category
General Purpose
Family
Spartan2
Device
XC2S15
Package
CS144
Speed
-6
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
ISE Simulator (VHDL/Verilog)
Enable Enhanced Design Summary
Enable Message Filtering
Display Incremental Messages
OK
Cancel
Default
Help
It will open a new window called Project Properties.
Transcript
Console
Errors
Warnings
Find in Files
CAPS NUM SCRL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
8:17 PM

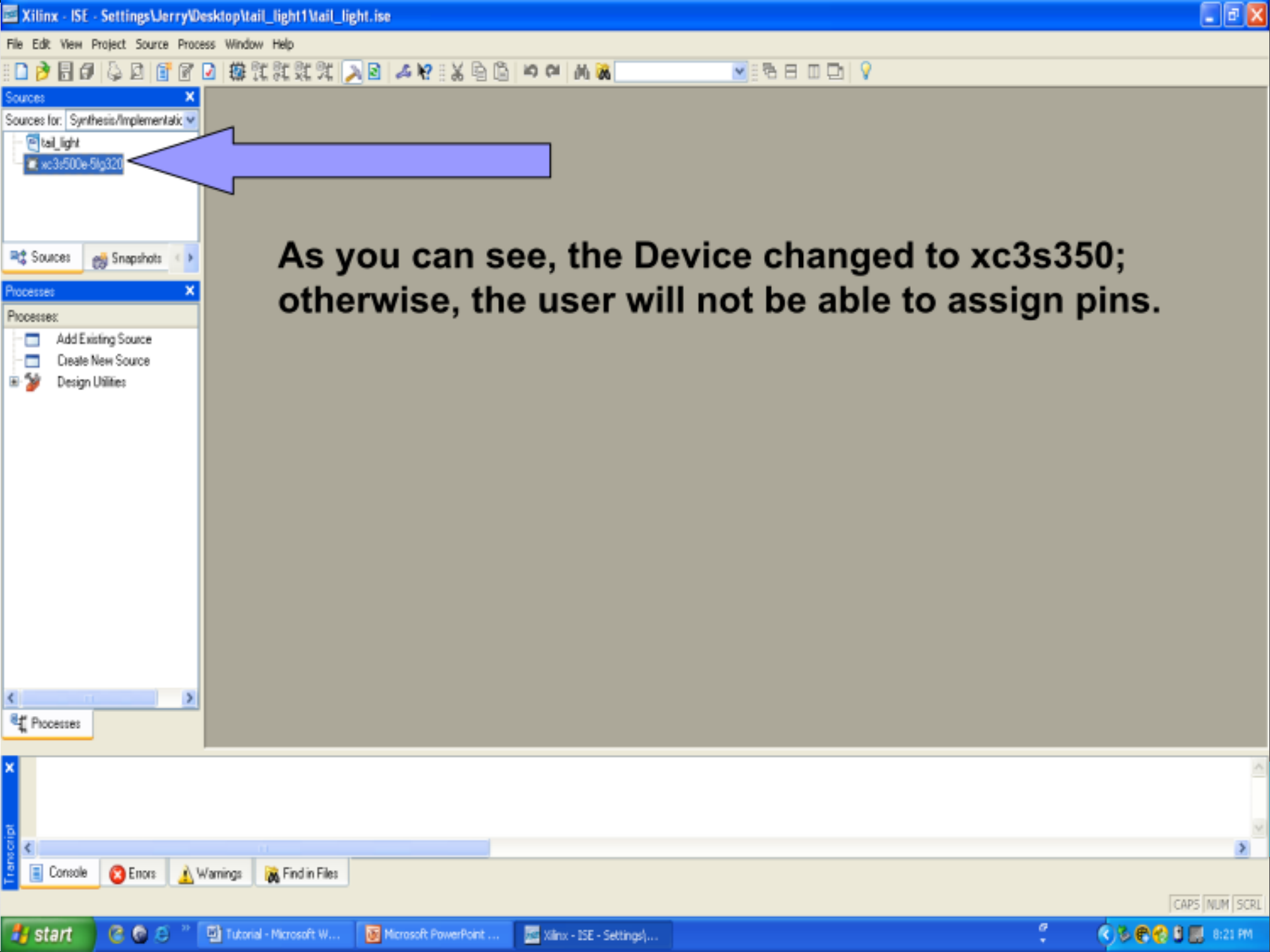

Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementation
tail_light
Sources
Snapshots
Processes
Processes:
Add Existing Source
Create New Source
Design Utilities
Processes
Project Properties
Property Name
Value
Product Category
General Purpose
Family
Spartan2
Device
Package
Speed
Top-Level Source Type
Synthesis Tool
Simulator
Spartan2
Spartan2E
Spartan3
Spartan3E
Virtex
Virtex2
Virtex2P
Virtex4
VirtexE
CoolRunner2 CPLDs
Enable Enhanced Design Summary
Enable Message Filtering
Display Incremental Messages
OK
Cancel
Default
Help
Select the Spartan-3E from the drop down menu.
Transcript
Console
Errors
Warnings
Find in Files
CAPS
NUM
SCRL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
8:18 PM

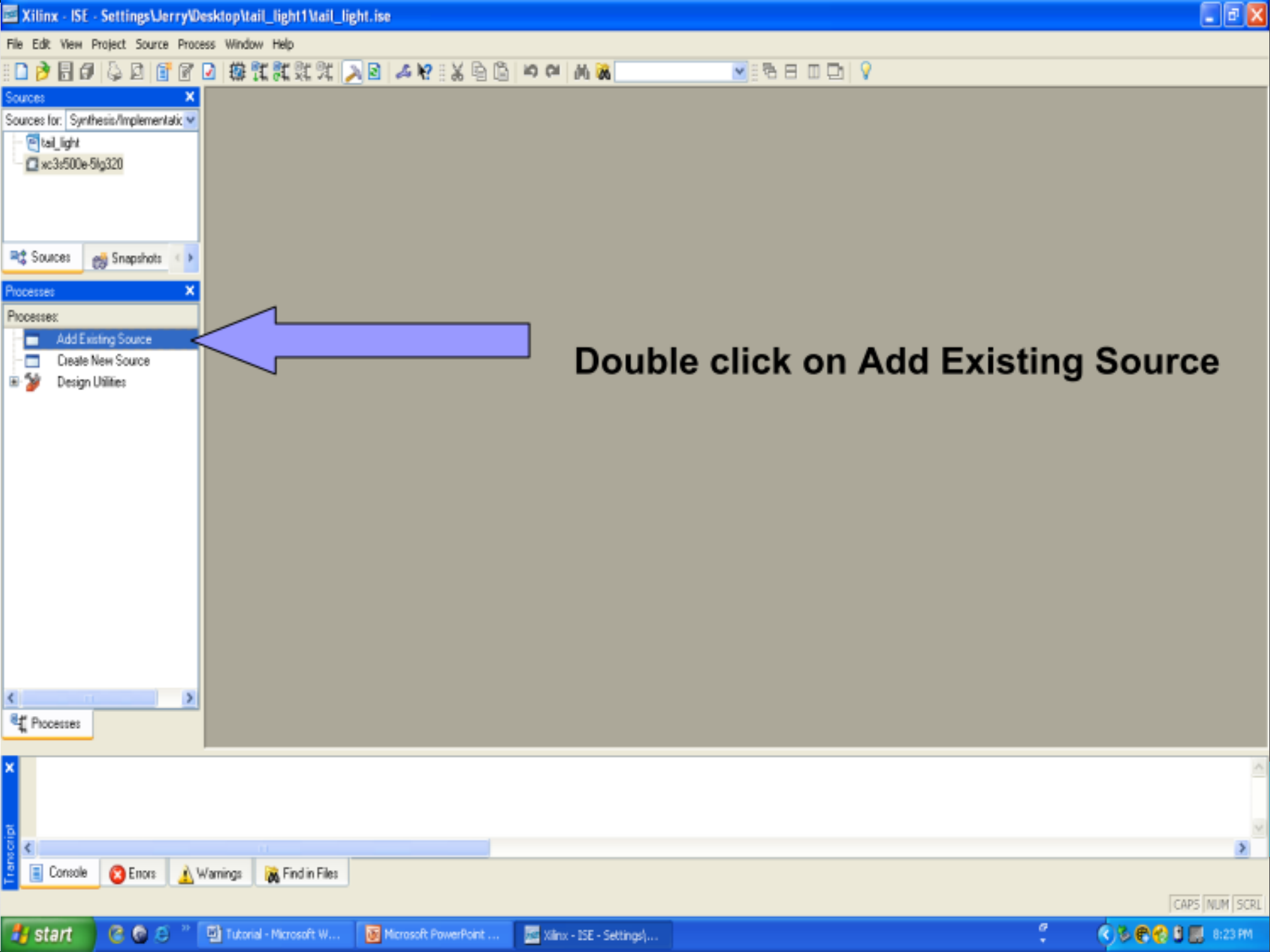

Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementation
tail_light
Sources
Snapshots
Processes
Processes:
Add Existing Source
Create New Source
Design Utilities
Processes
Project Properties
Property Name
Value
Product Category
General Purpose
Family
Spartan3E
Device
XC3S100E
Package
Speed
Top-Level Source Type
Synthesis Tool
XST (VHDL/Verilog)
Simulator
ISE Simulator (VHDL/Verilog)
Enable Enhanced Design Summary
Enable Message Filtering
Display Incremental Messages
OK
Cancel
Default
Help
XC3S100E
XC3S250E
XC3S500E
XC3S1200E
XC3S1600E
For the Device select (XC3S350E)
Transcript
Console
Errors
Warnings
Find in Files
CAPS NUM SCRL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
8:19 PM

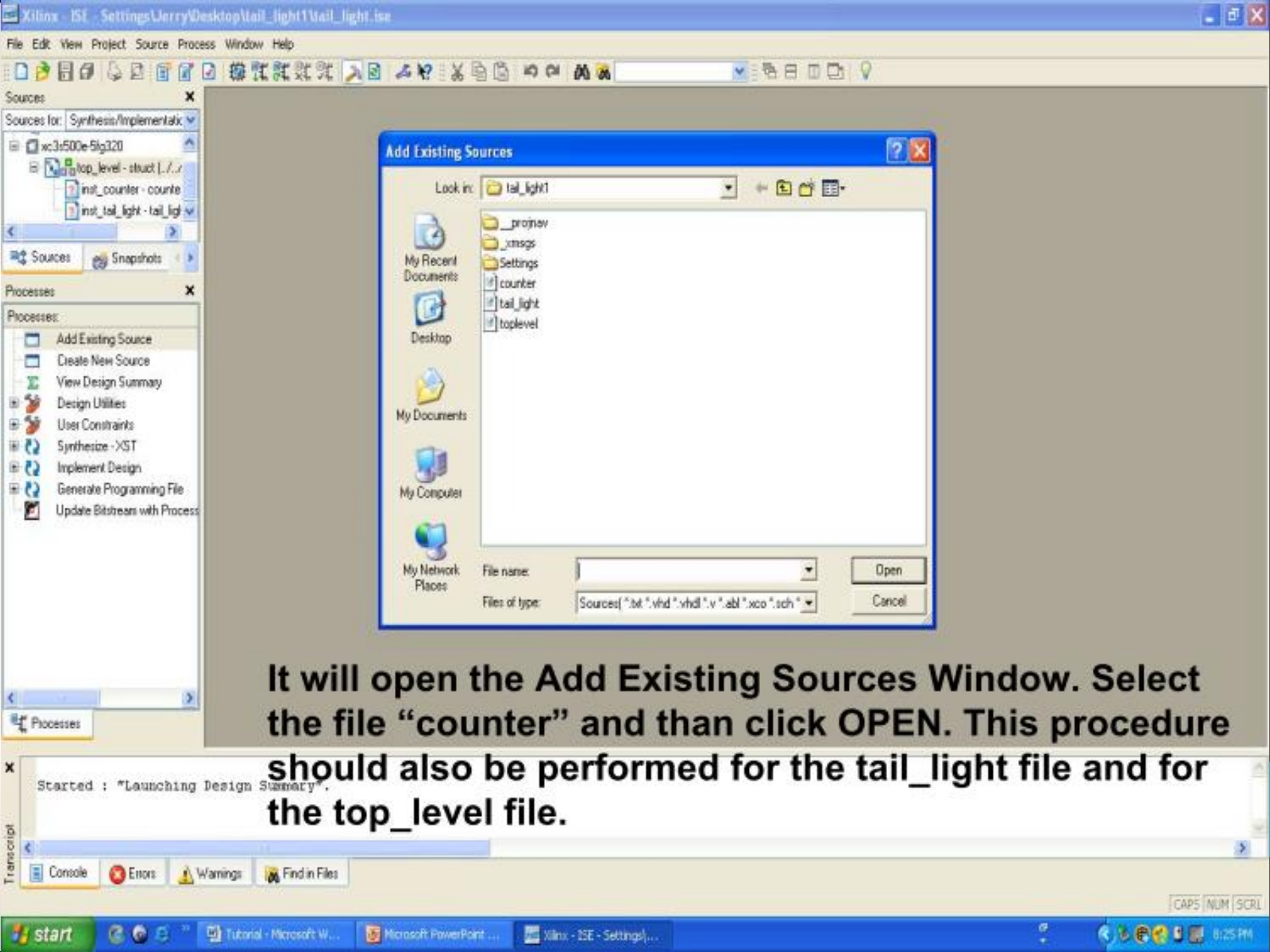

Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementation
tail_light
Sources
Snapshots
Processes
Processes:
Add Existing Source
Create New Source
Design Utilities
Processes
Project Properties
Property Name
Value
Product Category
General Purpose
Family
Spartan3E
Device
XC3S500E
Package
CP132
Speed
CP132
FT256
FG320
PQ208
Top-Level Source Type
Synthesis Tool
Simulator
ISE Simulator (VHDL/Verilog)
Enable Enhanced Design Summary
Enable Message Filtering
Display Incremental Messages
OK
Cancel
Default
Help
For the Package select (FG320)
Transcript
Console
Errors
Warnings
Find in Files
CAPS NUM SCRL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
8:20 PM


Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementation
tail_light
Sources
Snapshots
Processes
Processes:
Add Existing Source
Create New Source
Design Utilities
Processes
Project Properties
Property Name
Value
Product Category
General Purpose
Family
Spartan3E
Device
XC3S500E
Package
FG320
Speed
-5
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
ISE Simulator (VHDL/Verilog)
Enable Enhanced Design Summary
Enable Message Filtering
Display Incremental Messages
OK
Cancel
Default
Help
For the Speed use the default -5.
Transcript
Console
Errors
Warnings
Find in Files
CAPS NUM SCRL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
8:20 PM

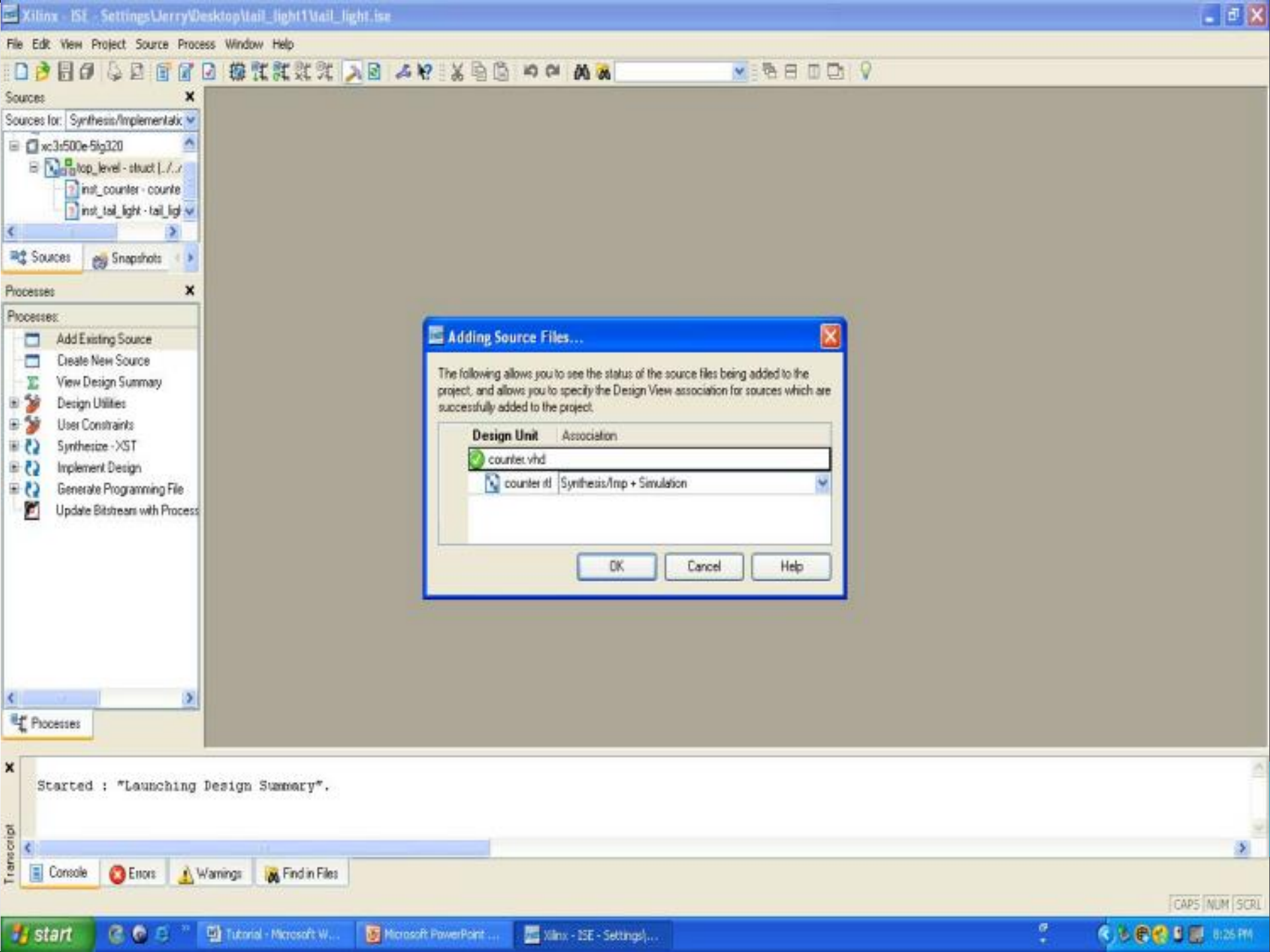

Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementation
tail_light
Sources
Snapshots
Processes
Processes:
Add Existing Source
Create New Source
Design Utilities
Processes
Project Properties
Property Name
Value
Product Category
General Purpose
Family
Spartan3E
Device
XC3S500E
Package
FG320
Speed
-5
Top-Level Source Type
HDL
Synthesis Tool
XST (VHDL/Verilog)
Simulator
ISE Simulator (VHDL/Verilog)
Enable Enhanced Design Summary
Enable Message Filtering
Display Incremental Messages
OK
Transcript
Console
Errors
Warnings
Find in Files
CAPS NUM SCRL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
8:20 PM

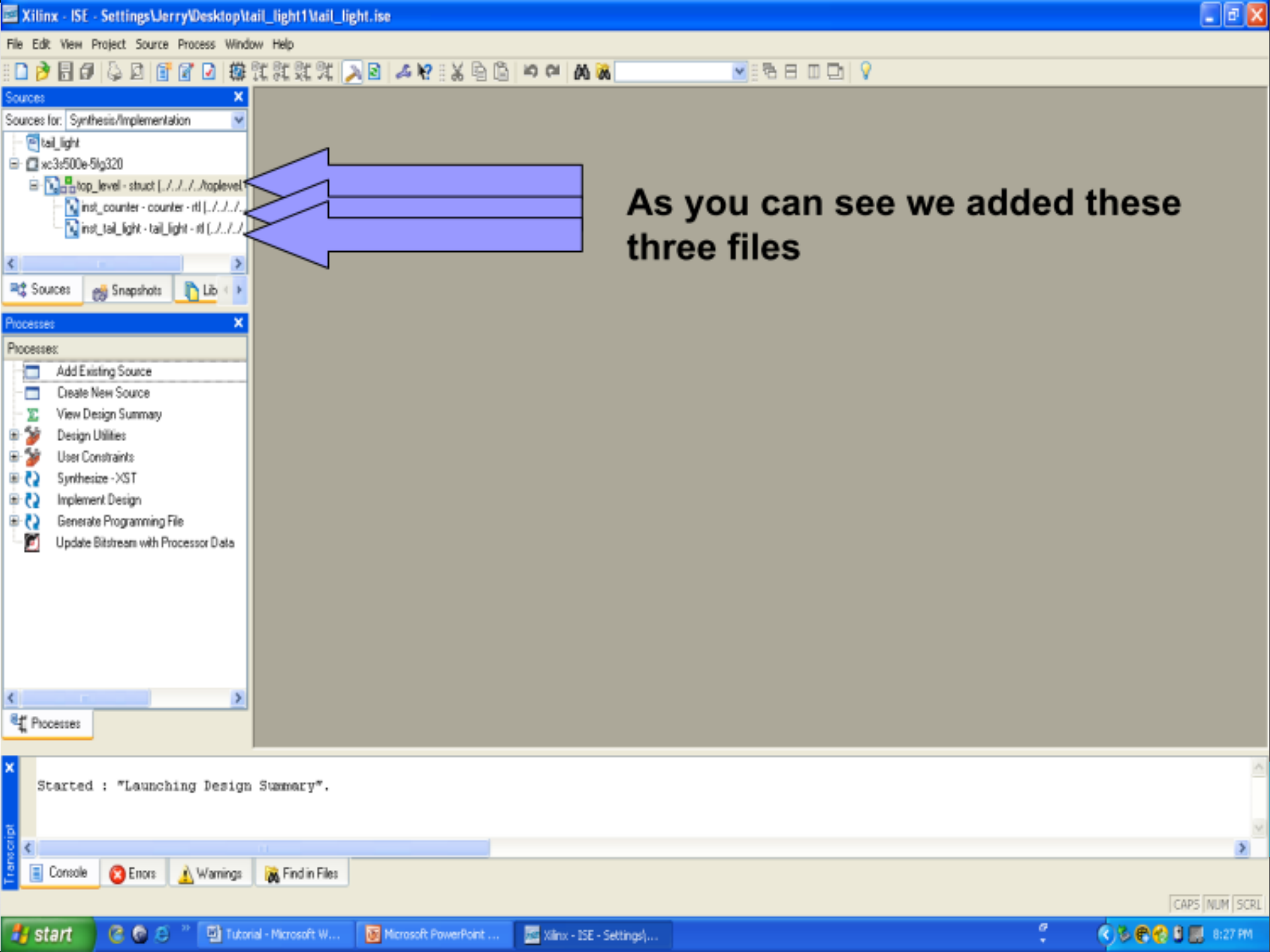

Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementatic
tail_light
xc3s500e-5fg320
Sources
Snapshots
Processes
Processes:
Add Existing Source
Create New Source
Design Utilities
Processes
As you can see, the Device changed to xc3s350;
otherwise, the user will not be able to assign pins.
Transcript
Console
Errors
Warnings
Find in Files
CAPS NUM SCRL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
8:21 PM

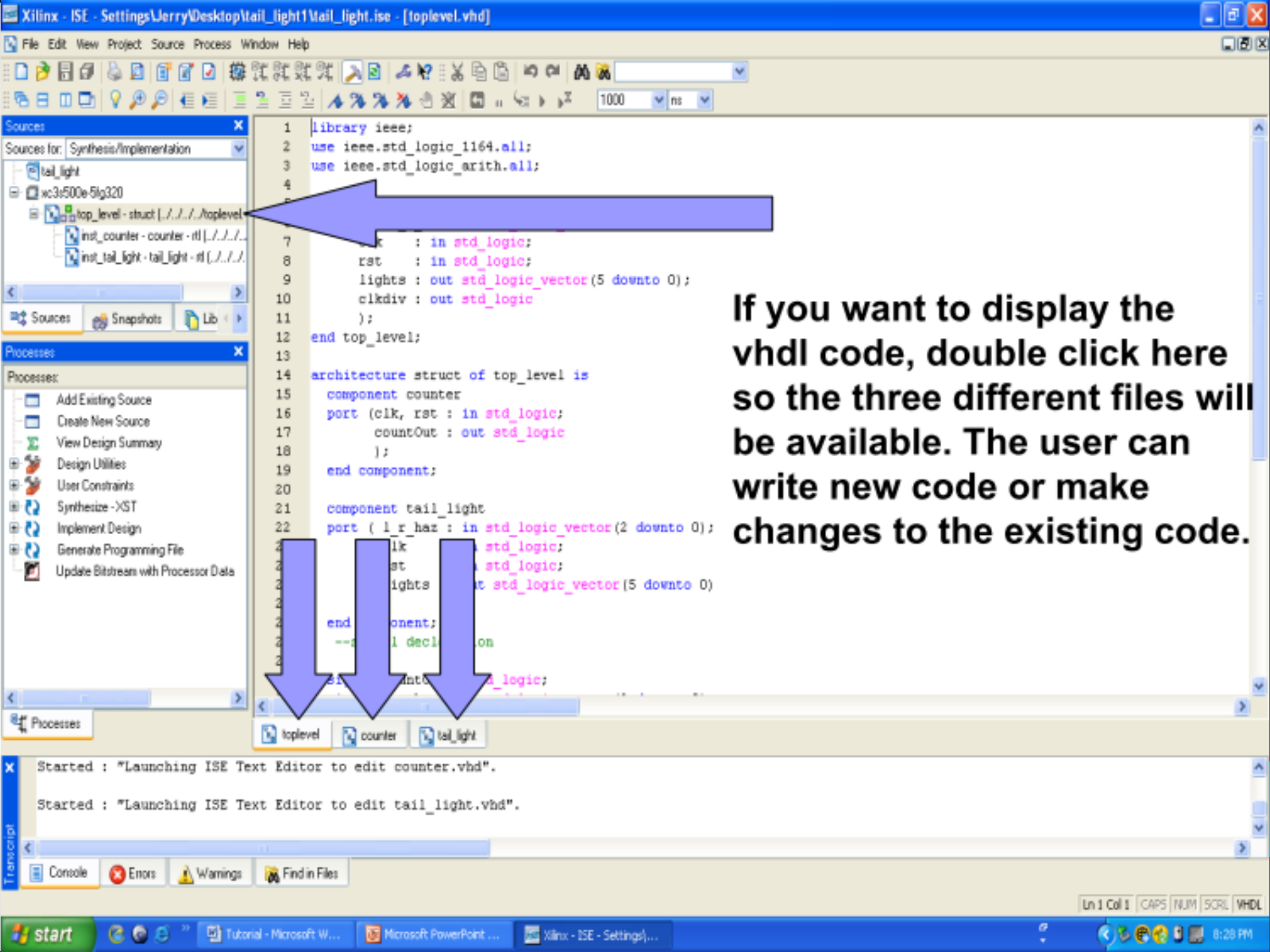

Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementatic
tail_light
xc3s500e-5fg320
Sources
Snapshots
Processes
Processes:
Add Existing Source
Create New Source
Design Utilities
Processes
Double click on Add Existing Source
Transcript
Console
Errors
Warnings
Find in Files
CAPS NUM SCRL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
8:23 PM



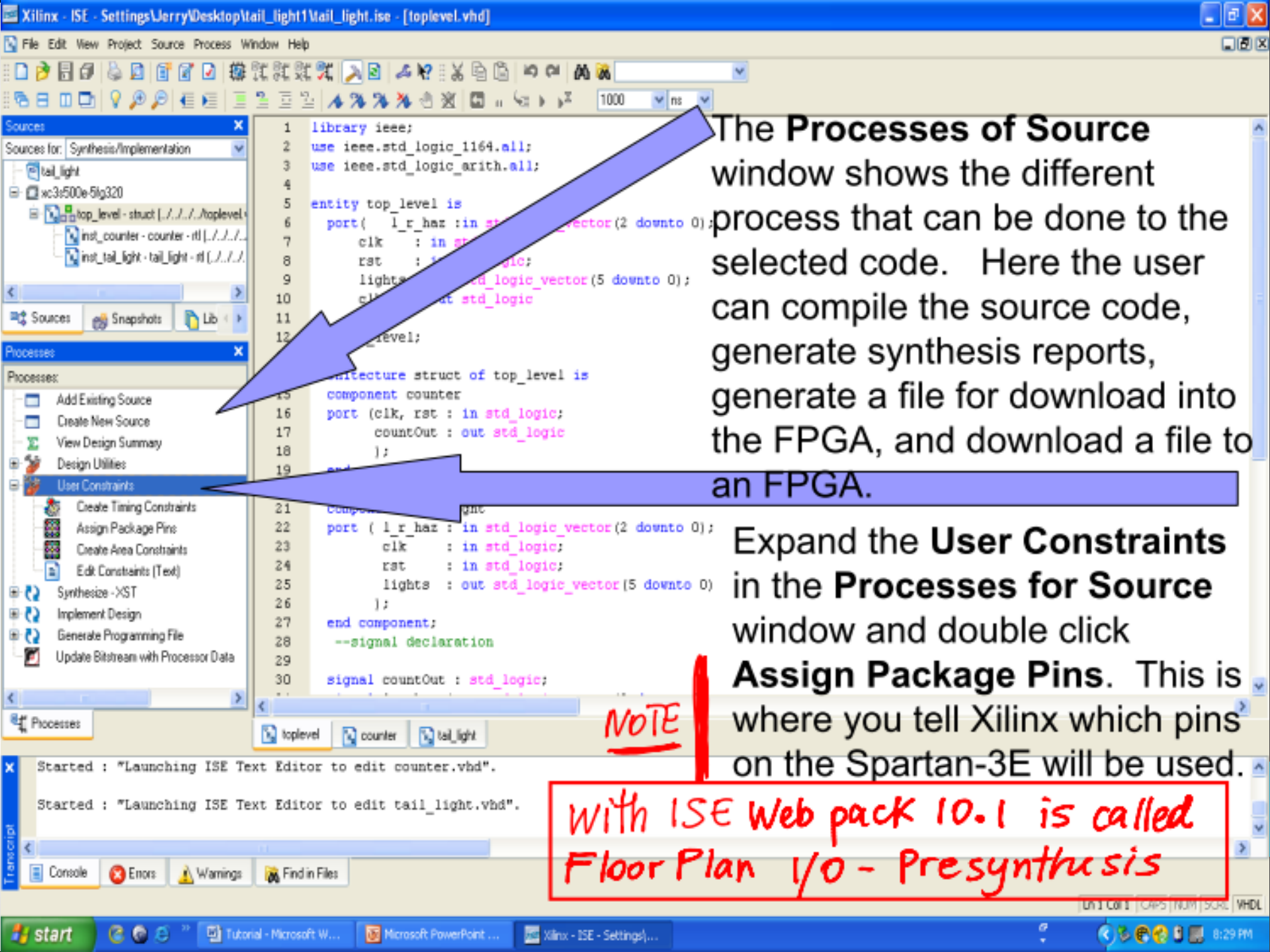
It will open the Add Existing Sources Window. Select the file “counter” and than click OPEN. This procedure should also be performed for the tail_light file and for the top_level file.


Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementatic
xc3s500e-5fg320
top_level - struct [../..
inst_counter - counte
inst_tail_light - tail_ligl
Sources
Snapshots
Processes
Processes:
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Update Bitstream with Process
Processes
Adding Source Files...
The following allows you to see the status of the source files being added to the project, and allows you to specify the Design View association for sources which are successfully added to the project.
Design Unit
Association
counter.vhd
counter (t
Synthesis/Imp + Simulation
OK
Cancel
Help
Started : "Launching Design Summary".
Transcript
Console
Errors
Warnings
Find in Files
CAPS NUM SCRL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
8:26 PM


Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementation
tail_light
xc3s500e-5fg320
top_level - struct (../../../../toplevel
inst_counter - counter - rtl (../../../
inst_tail_light - tail_light - rtl (../../../
Sources
Snapshots
Lib
Processes
Processes:
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Update Bitstream with Processor Data
Processes
As you can see we added these three files
Started : "Launching Design Summary".
Transcript
Console
Errors
Warnings
Find in Files
CAPS NUM SCRL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
8:27 PM



If you want to display the vhdl code, double click here so the three different files will be available. The user can write new code or make changes to the existing code.

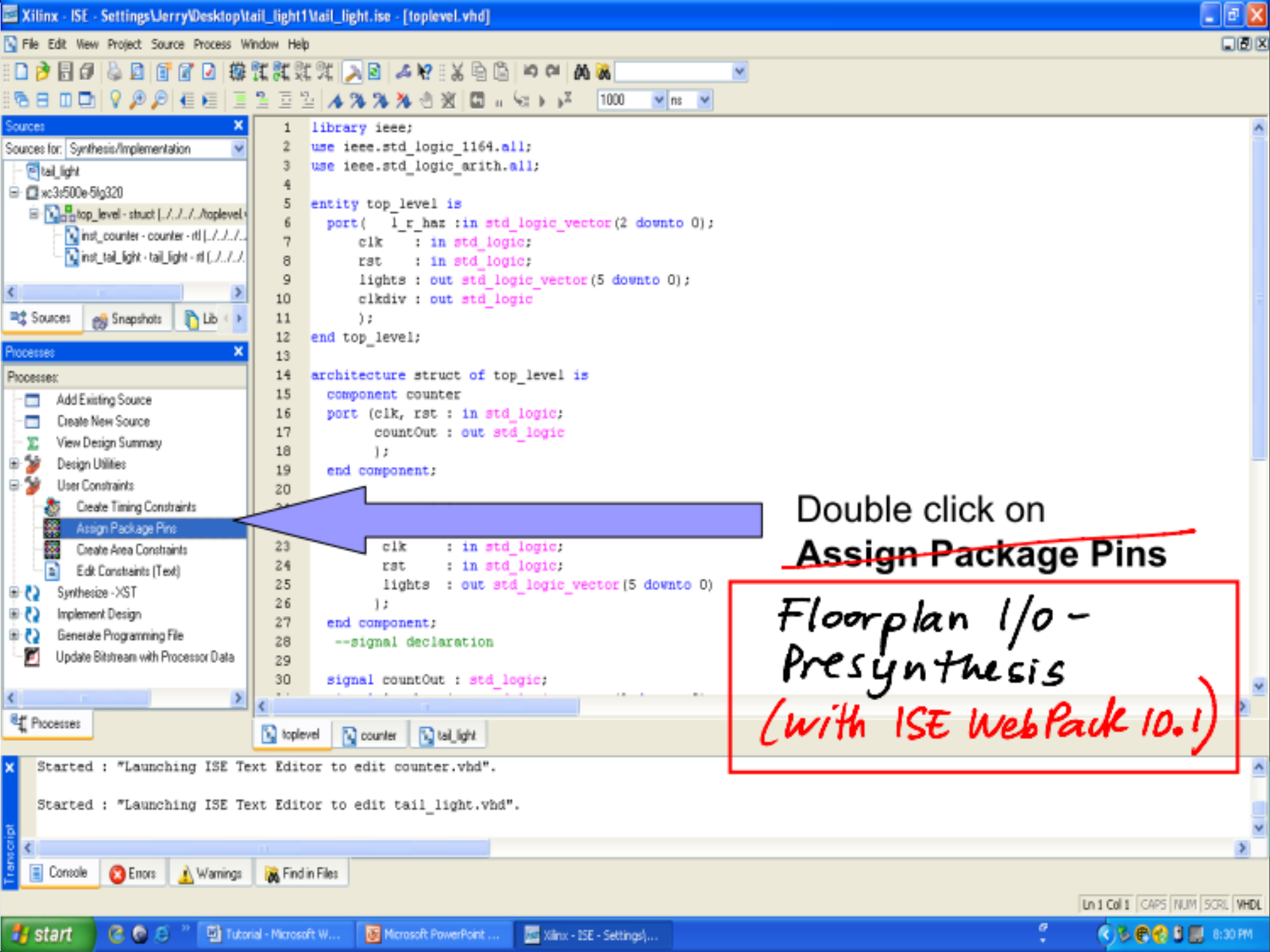


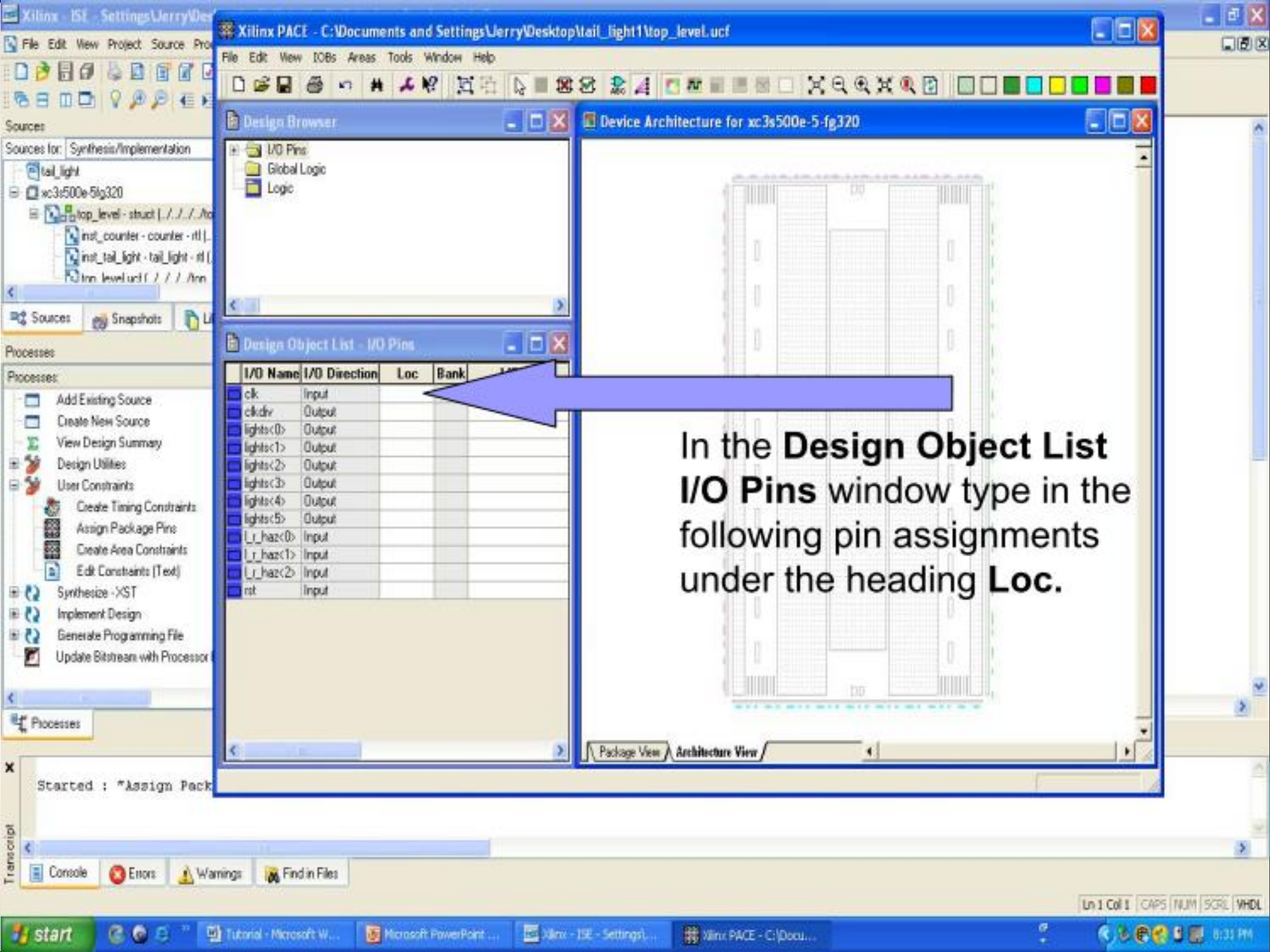
The **Processes of Source** window shows the different process that can be done to the selected code. Here the user can compile the source code, generate synthesis reports, generate a file for download into the FPGA, and download a file to an FPGA.

Expand the **User Constraints** in the **Processes for Source** window and double click **Assign Package Pins**. This is where you tell Xilinx which pins on the Spartan-3E will be used.

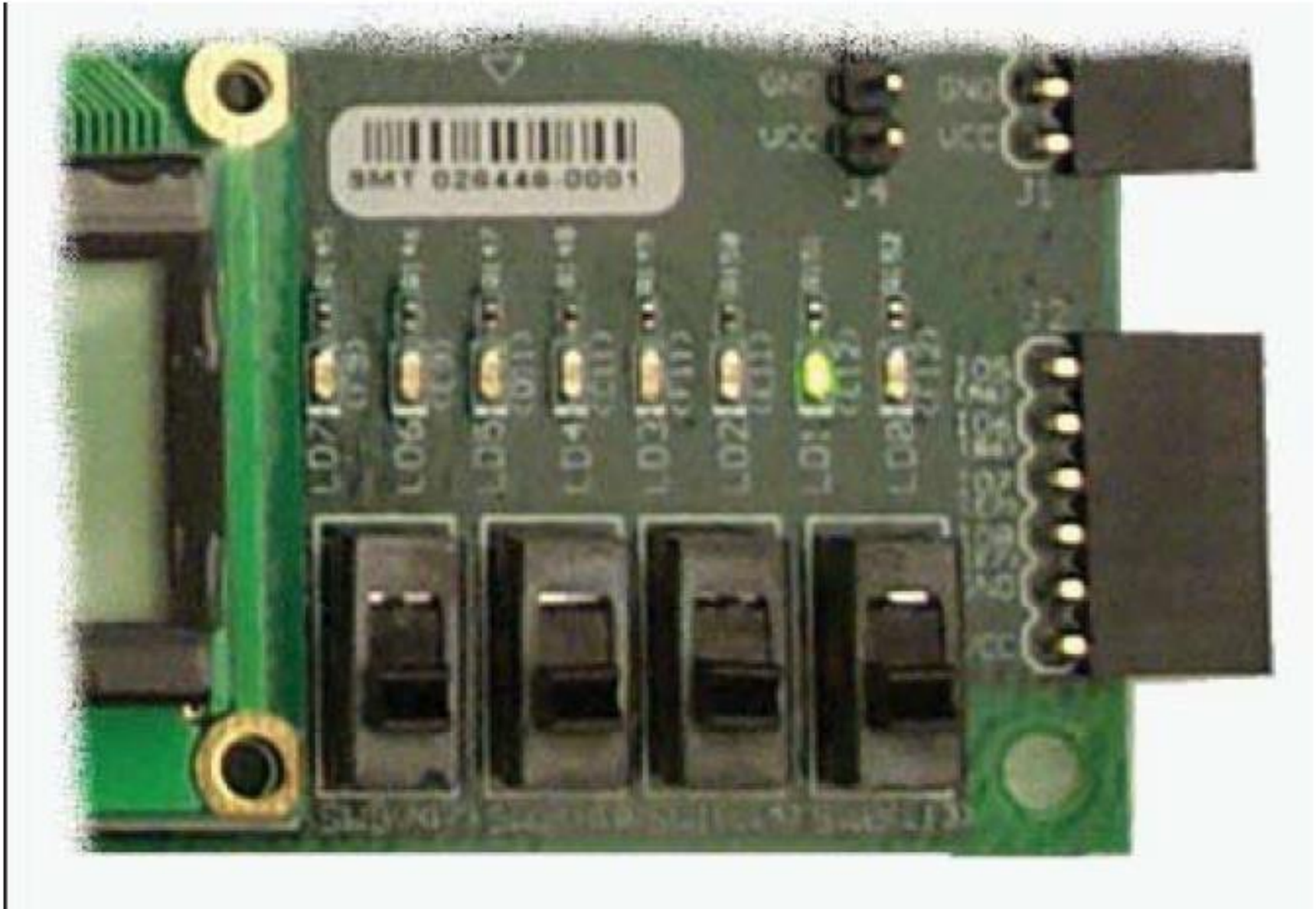
NOTE

with ISE Web pack 10.1 is called Floor Plan I/O - Presynthesis


Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise - [toplevel.vhd]
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementation
tail_light
xc3s500e-5fg320
top_level - struct (../../../toplevel.v
inst_counter - counter - rtl (../../../
inst_tail_light - tail_light - rtl (../../../
Sources
Snapshots
Lib
Processes
Processes:
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Create Timing Constraints
Assign Package Pins
Create Area Constraints
Edit Constraints (Text)
Synthesize - XST
Implement Design
Generate Programming File
Update Bitstream with Processor Data
Processes
1 library ieee;
2 use ieee.std_logic_1164.all;
3 use ieee.std_logic_arith.all;
4
5 entity top_level is
6 port(l_r_haz :in std_logic_vector(2 downto 0);
7 clk : in std_logic;
8 rst : in std_logic;
9 lights : out std_logic_vector(5 downto 0);
10 clkdiv : out std_logic
11);
12 end top_level;
13
14 architecture struct of top_level is
15 component counter
16 port (clk, rst : in std_logic;
17 countOut : out std_logic
18);
19 end component;
20
23 clk : in std_logic;
24 rst : in std_logic;
25 lights : out std_logic_vector(5 downto 0)
26);
27 end component;
28 --signal declaration
29
30 signal countOut : std_logic;
toplevel
counter
tail_light
Double click on
Assign Package Pins
Floorplan I/O -
Presynthesis
(with ISE WebPack 10.1)
Started : "Launching ISE Text Editor to edit counter.vhd".
Started : "Launching ISE Text Editor to edit tail_light.vhd".
Transcript
Console
Errors
Warnings
Find in Files
Ln 1 Col 1
CAPS
NUM
SCRL
VHDL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
8:30 PM

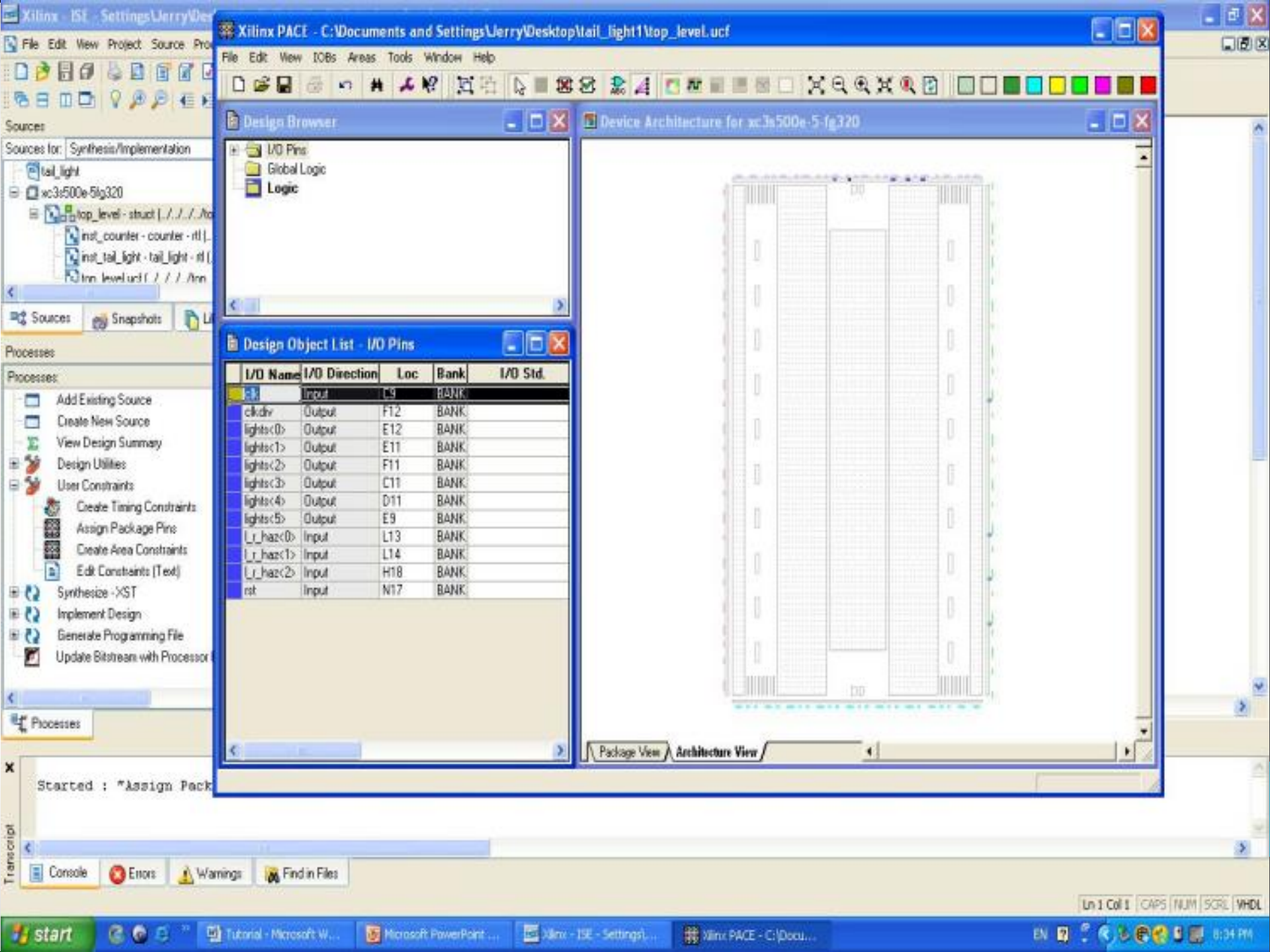

Xilinx PACE - C:\Documents and Settings\Jerry\Desktop\tail_light1\top_level.ucf
File Edit View IOBs Areas Tools Window Help
Design Browser
I/O Pins
Global Logic
Logic
Design Object List - I/O Pins
I/O Name
I/O Direction
Loc
Bank
clk Input
clk:div Output
lights<0> Output
lights<1> Output
lights<2> Output
lights<3> Output
lights<4> Output
lights<5> Output
l_r_haz<0> Input
l_r_haz<1> Input
l_r_haz<2> Input
rst Input
Device Architecture for xc3s500e-5-fg320
Package View
Architecture View
In the Design Object List I/O Pins window type in the following pin assignments under the heading Loc.

Four Slide Switches

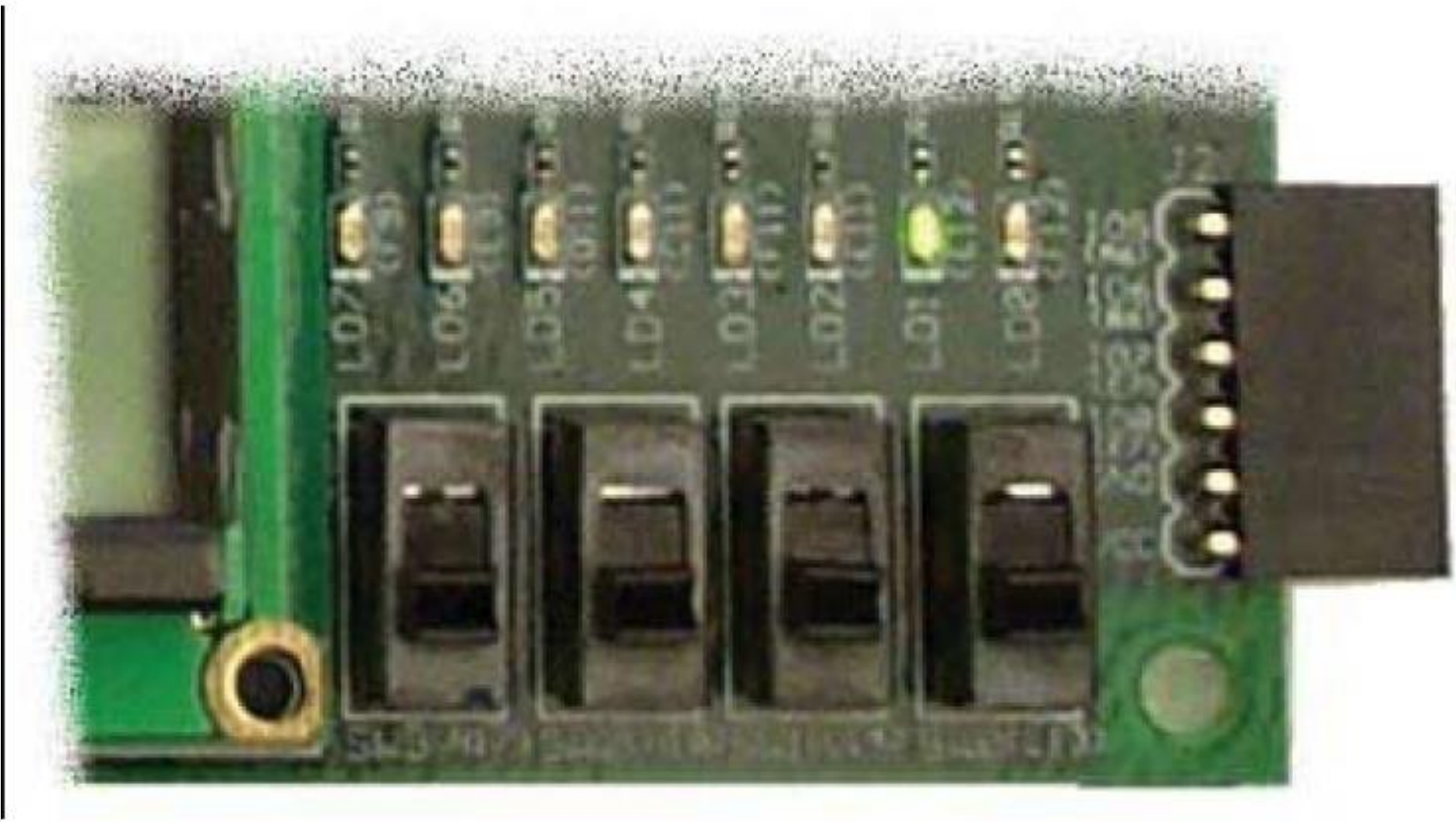


Pin assignments

- NET "SW<0>" LOC = "L13" | IOSTANDARD = LVTTL | PULLUP ;
- NET "SW<1>" LOC = "L14" | IOSTANDARD = LVTTL | PULLUP ;
- NET "SW<2>" LOC = "H18" | IOSTANDARD = LVTTL | PULLUP ;
- NET "SW<3>" LOC = "N17" | IOSTANDARD = LVTTL | PULLUP ;

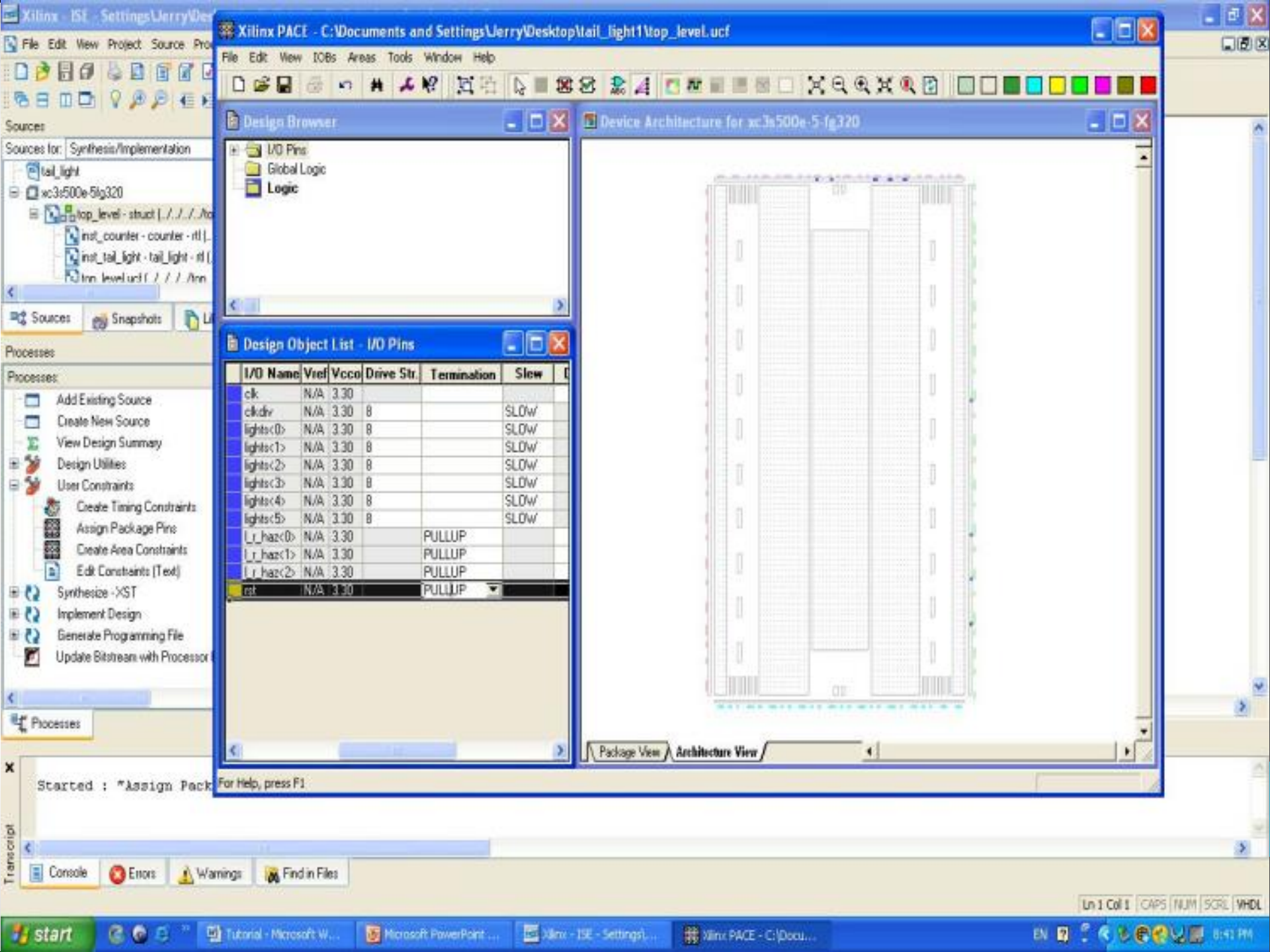

Xilinx PACE - C:\Documents and Settings\Jerry\Desktop\tail_light1\top_level.ucf
File Edit View IOBs Areas Tools Window Help
Design Browser
I/O Pins
Global Logic
Logic
Device Architecture for xc3s500e-5-fg320
Package View
Architecture View
Design Object List - I/O Pins
I/O Name | I/O Direction | Loc | Bank | I/O Std.
clk | Input | C9 | BANK
clkdiv | Output | F12 | BANK
lights<0> | Output | E12 | BANK
lights<1> | Output | E11 | BANK
lights<2> | Output | F11 | BANK
lights<3> | Output | C11 | BANK
lights<4> | Output | D11 | BANK
lights<5> | Output | E9 | BANK
l_r_haz<0> | Input | L13 | BANK
l_r_haz<1> | Input | L14 | BANK
l_r_haz<2> | Input | H18 | BANK
rst | Input | N17 | BANK
Sources
Sources for: Synthesis/Implementation
tail_light
xc3s500e-5fg320
Processes
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Create Timing Constraints
Assign Package Pins
Create Area Constraints
Edit Constraints (Text)
Synthesize - XST
Implement Design
Generate Programming File
Update Bitstream with Processor
Started : "Assign Pack
Console
Errors
Warnings
Find in Files
Transcript
start

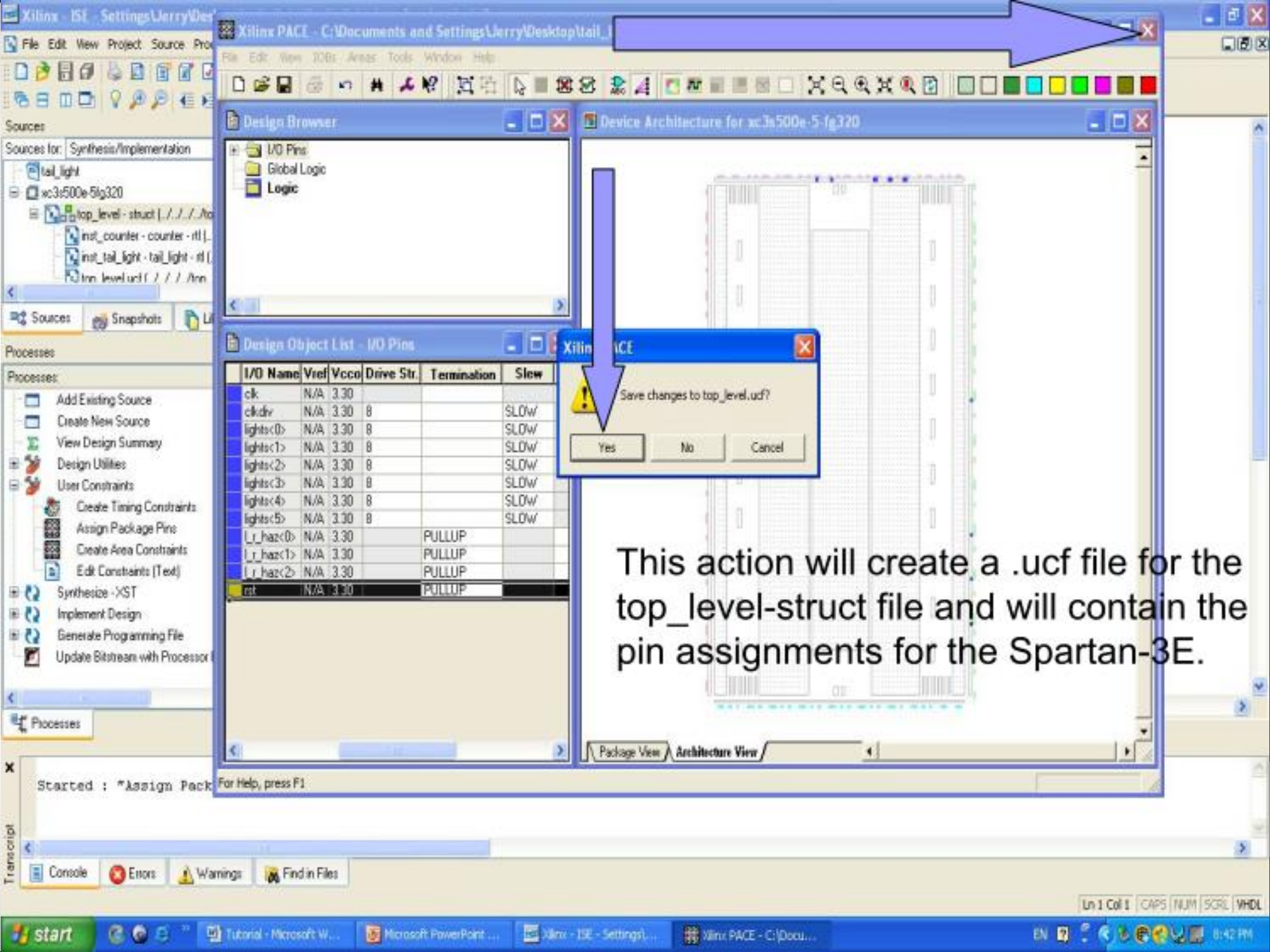
Eight Discrete LEDs

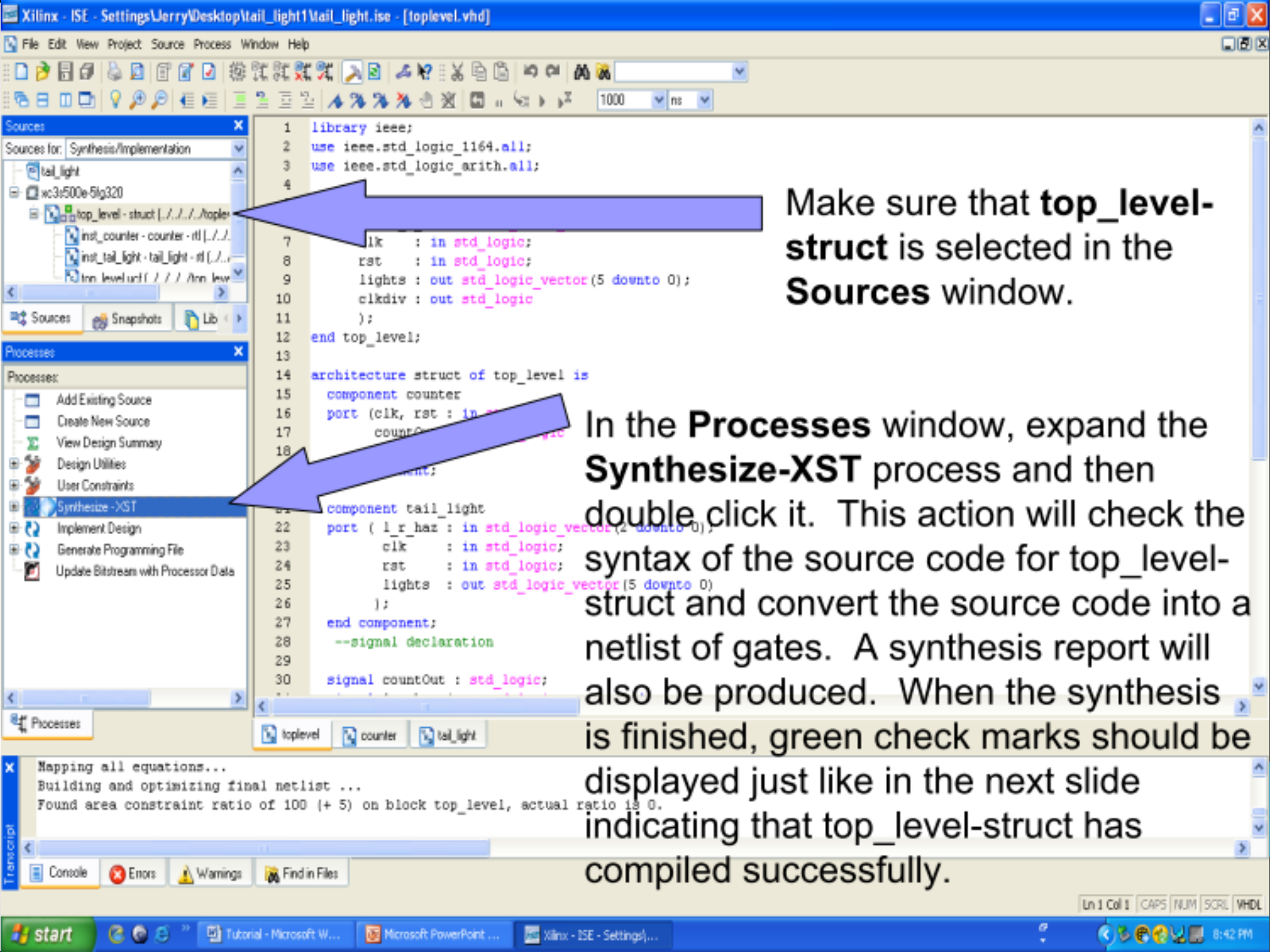


UCF Constraints for Eight Discrete LEDs

- NET "LED<7>" LOC = "F9" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
- NET "LED<6>" LOC = "E9" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
- NET "LED<5>" LOC = "D11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
- NET "LED<4>" LOC = "C11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
- NET "LED<3>" LOC = "F11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
- NET "LED<2>" LOC = "E11" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
- NET "LED<1>" LOC = "E12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;
- NET "LED<0>" LOC = "F12" | IOSTANDARD = LVTTL | SLEW = SLOW | DRIVE = 8 ;

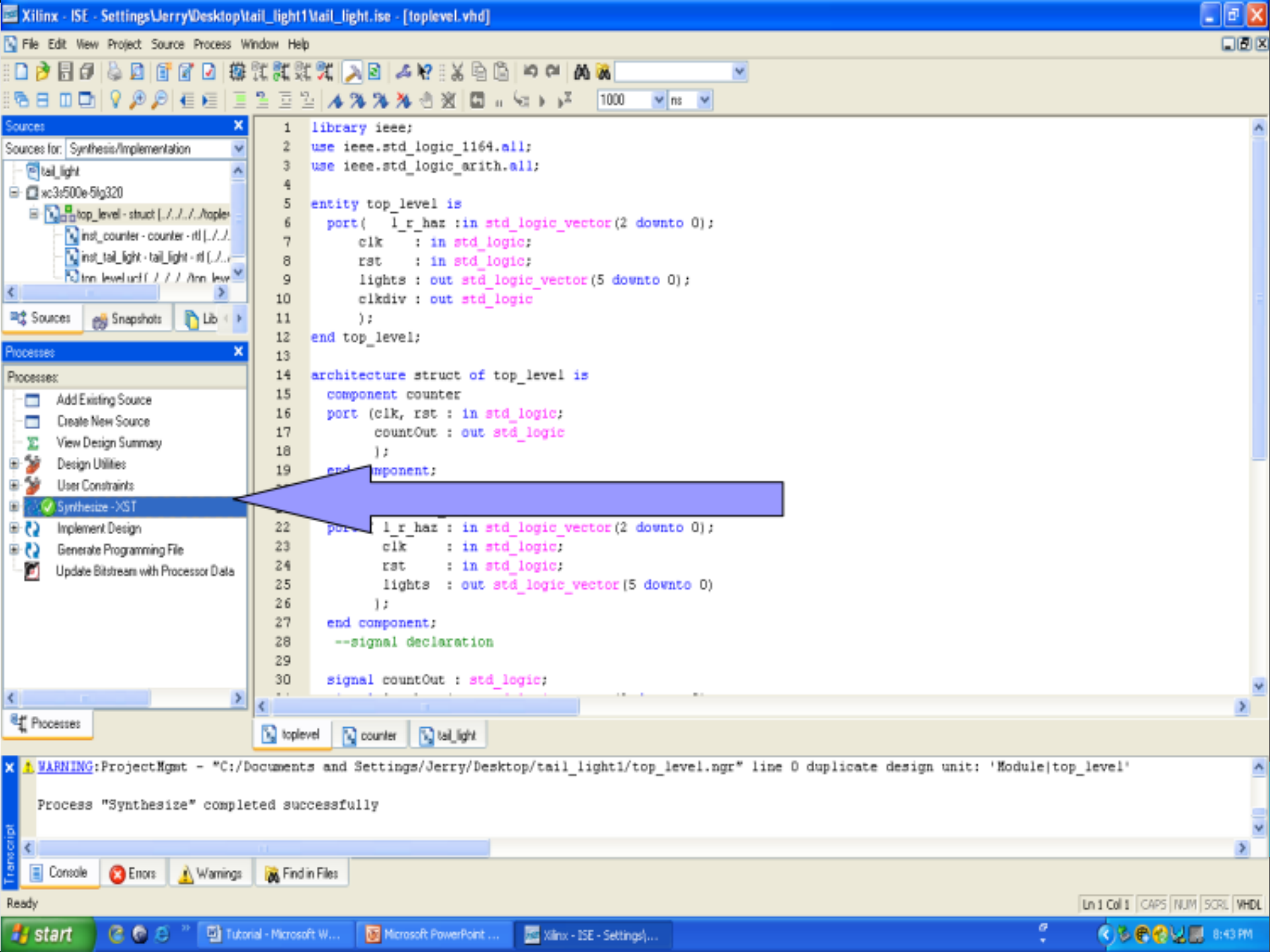

Xilinx PACE - C:\Documents and Settings\Jerry\Desktop\tail_light1\top_level.ucf
File Edit View IOBs Areas Tools Window Help
Design Browser
I/O Pins
Global Logic
Logic
Device Architecture for xc3s500e-5-fg320
Design Object List - I/O Pins
I/O Name Vref Vcco Drive Str. Termination Slew
clk N/A 3.30
clkdiv N/A 3.30 8 SLOW
lights<0> N/A 3.30 8 SLOW
lights<1> N/A 3.30 8 SLOW
lights<2> N/A 3.30 8 SLOW
lights<3> N/A 3.30 8 SLOW
lights<4> N/A 3.30 8 SLOW
lights<5> N/A 3.30 8 SLOW
l_r_haz<0> N/A 3.30 PULLUP
l_r_haz<1> N/A 3.30 PULLUP
l_r_haz<2> N/A 3.30 PULLUP
rst N/A 3.30 PULLUP
Package View
Architecture View
For Help, press F1
Sources
Snapshots
Processes
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Create Timing Constraints
Assign Package Pins
Create Area Constraints
Edit Constraints (Text)
Synthesize - XST
Implement Design
Generate Programming File
Update Bitstream with Processor
Started : "Assign Pack
Console
Errors
Warnings
Find in Files
Transcript
Ln 1 Col 1
CAPS
NUM
SCRL
VHDL
start

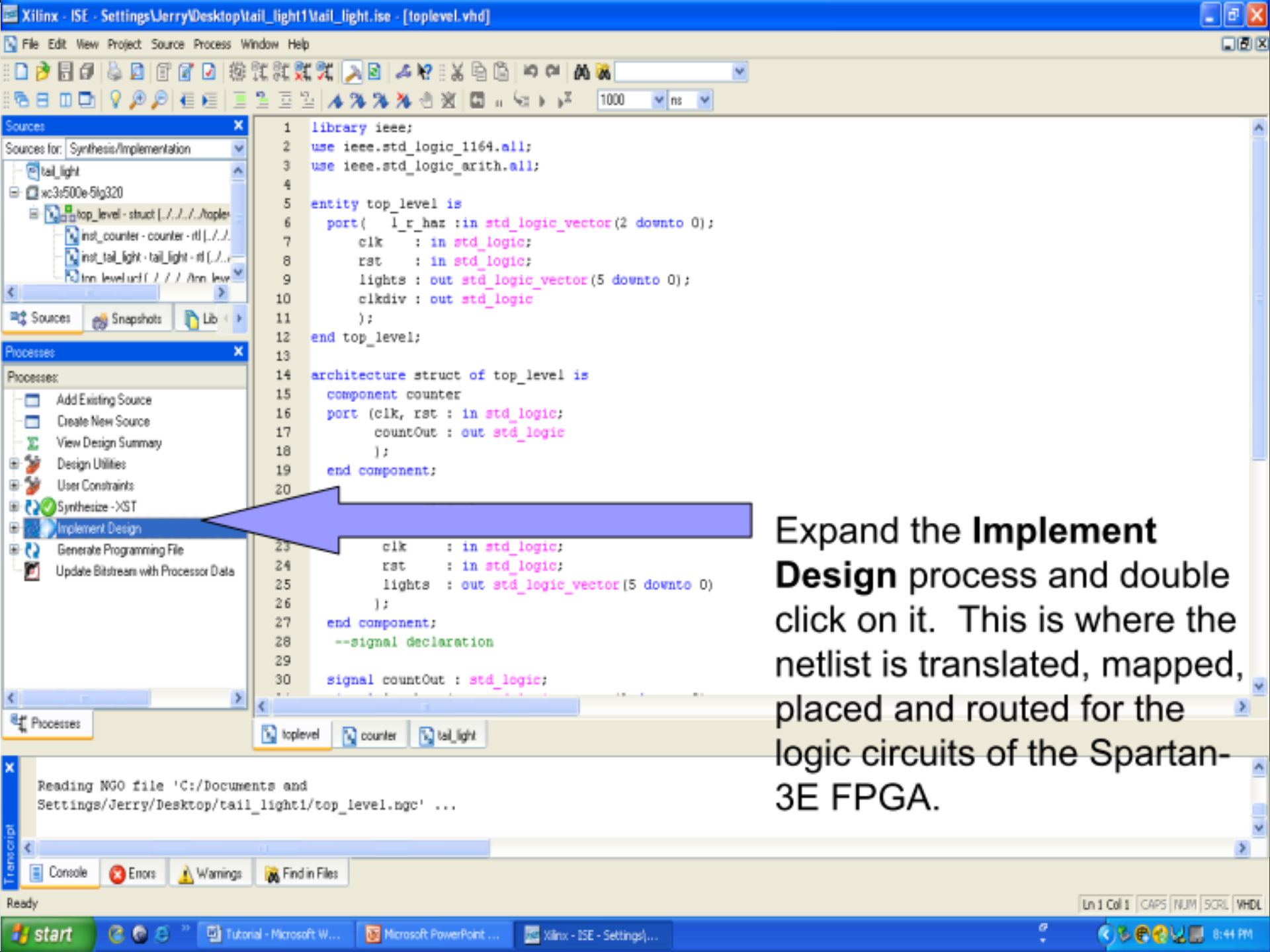

Xilinx PACE - C:\Documents and Settings\Jerry\Desktop\tail_l
Design Browser
I/O Pins
Global Logic
Logic
Device Architecture for xc3s500e-5-fg320
Design Object List - I/O Pins
I/O Name Vref Vcco Drive Str. Termination Slew
clk N/A 3.30 SLOW
clkdiv N/A 3.30 8 SLOW
lights<0> N/A 3.30 8 SLOW
lights<1> N/A 3.30 8 SLOW
lights<2> N/A 3.30 8 SLOW
lights<3> N/A 3.30 8 SLOW
lights<4> N/A 3.30 8 SLOW
lights<5> N/A 3.30 8 SLOW
l_r_haz<0> N/A 3.30 PULLUP
l_r_haz<1> N/A 3.30 PULLUP
l_r_haz<2> N/A 3.30 PULLUP
rst N/A 3.30 PULLUP
Save changes to top_level.ucf?
Yes
No
Cancel
Package View
Architecture View
For Help, press F1
This action will create a .ucf file for the top_level-struct file and will contain the pin assignments for the Spartan-3E.



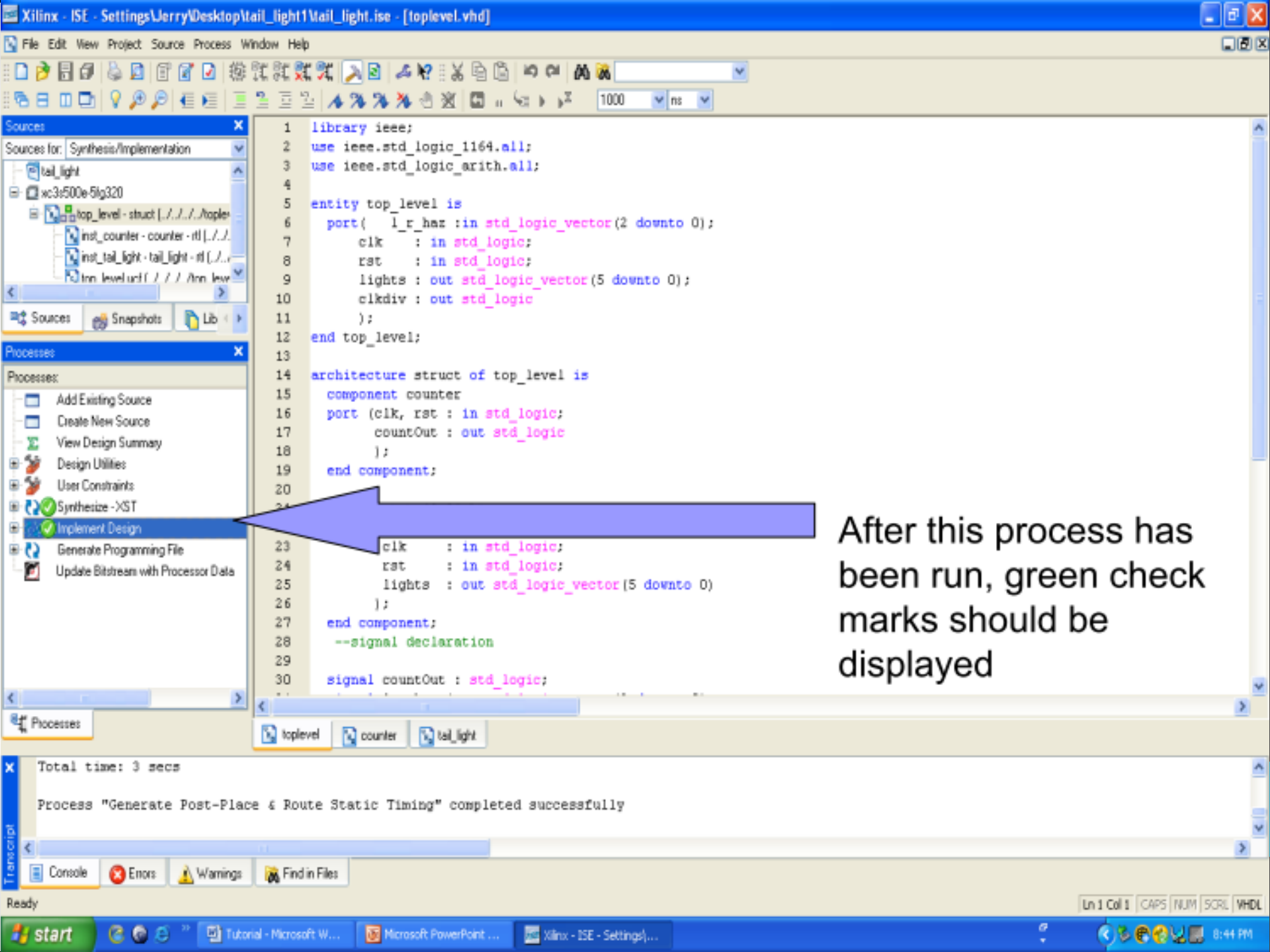
Make sure that **top_level-struct** is selected in the **Sources** window.

In the **Processes** window, expand the **Synthesize-XST** process and then double click it. This action will check the syntax of the source code for top_level-struct and convert the source code into a netlist of gates. A synthesis report will also be produced. When the synthesis is finished, green check marks should be displayed just like in the next slide indicating that top_level-struct has compiled successfully.

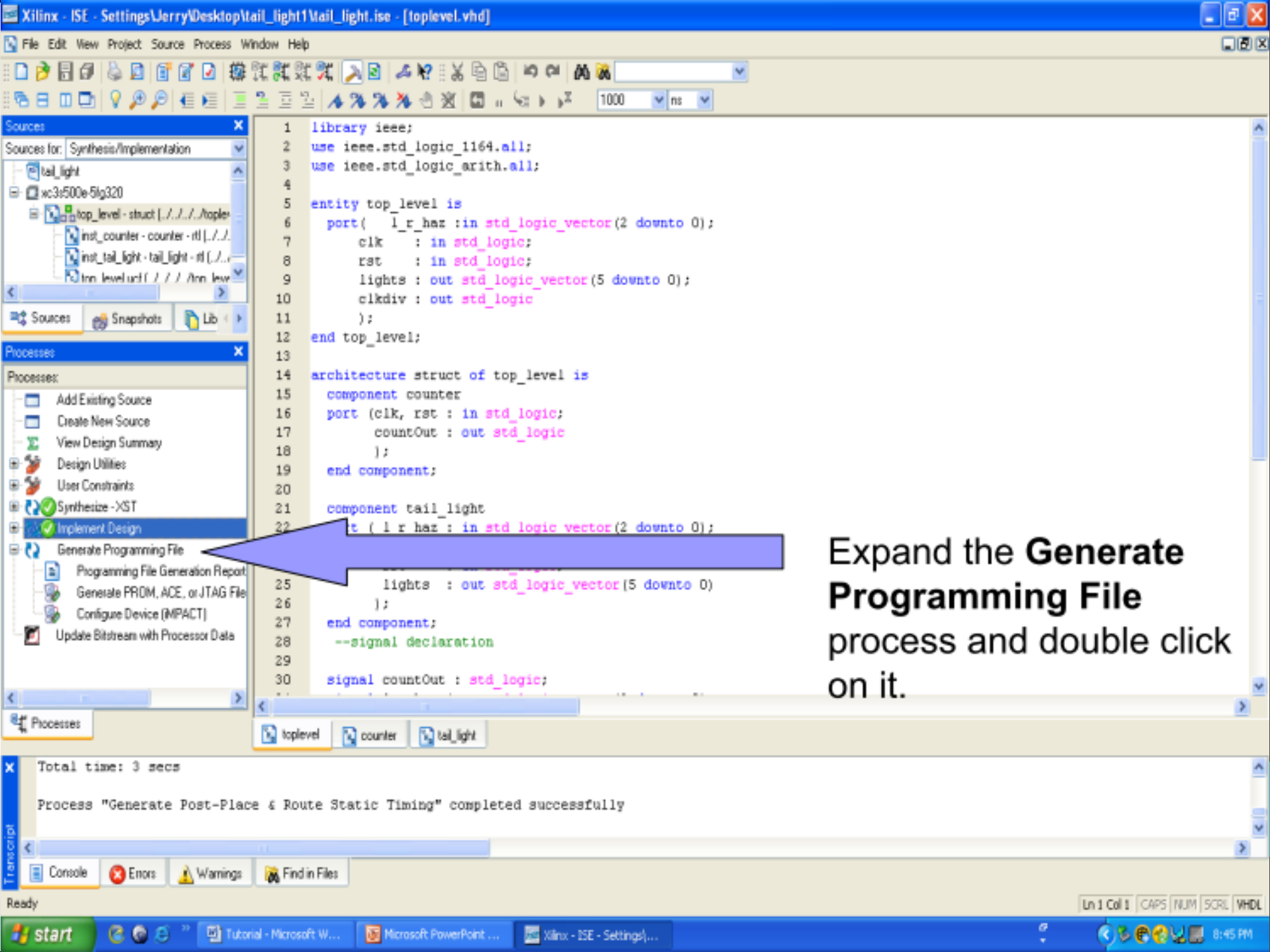

Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise - [toplevel.vhd]
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementation
tail_light
xc3s500e-5fg320
top_level - struct [../../../../toplev
inst_counter - counter - rtl [../../
inst_tail_light - tail_light - rtl [../..
Sources
Snapshots
Lib
Processes
Processes:
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Update Bitstream with Processor Data
Processes
1 library ieee;
2 use ieee.std_logic_1164.all;
3 use ieee.std_logic_arith.all;
4
5 entity top_level is
6 port(l_r_haz :in std_logic_vector(2 downto 0);
7 clk : in std_logic;
8 rst : in std_logic;
9 lights : out std_logic_vector(5 downto 0);
10 clkdiv : out std_logic
11);
12 end top_level;
13
14 architecture struct of top_level is
15 component counter
16 port (clk, rst : in std_logic;
17 countOut : out std_logic
18);
19 end component;
22 port(l_r_haz : in std_logic_vector(2 downto 0);
23 clk : in std_logic;
24 rst : in std_logic;
25 lights : out std_logic_vector(5 downto 0)
26);
27 end component;
28 --signal declaration
29
30 signal countOut : std_logic;
toplevel
counter
tail_light
WARNING:ProjectMgmt - "C:/Documents and Settings/Jerry/Desktop/tail_light1/top_level.ngr" line 0 duplicate design unit: 'Module|top_level'
Process "Synthesize" completed successfully
Transcript
Console
Errors
Warnings
Find in Files
Ready
Ln 1 Col 1
CAPS
NUM
SCRL
VHDL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
8:43 PM



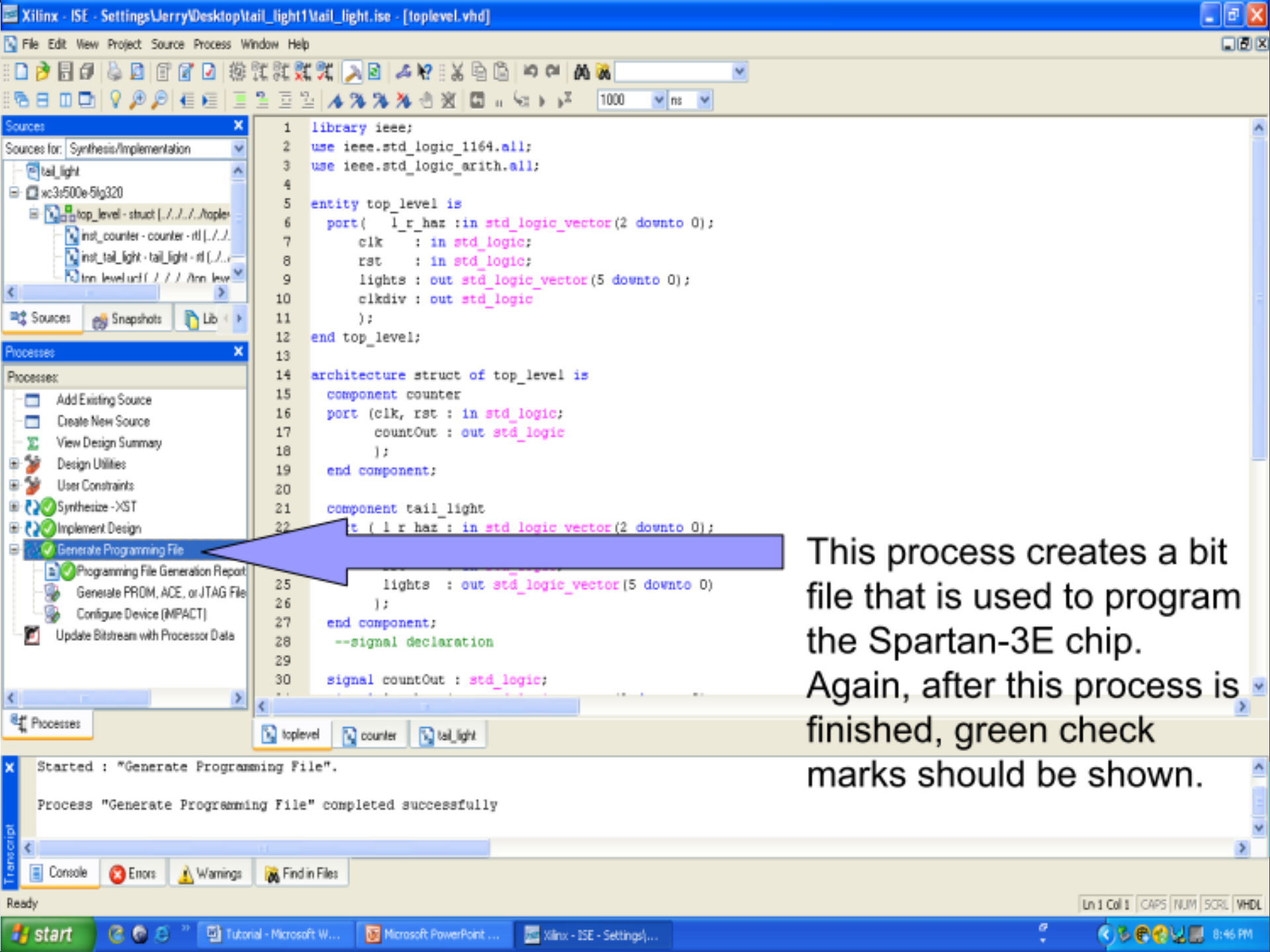
Expand the **Implement Design** process and double click on it. This is where the netlist is translated, mapped, placed and routed for the logic circuits of the Spartan-3E FPGA.



After this process has been run, green check marks should be displayed



Expand the **Generate Programming File** process and double click on it.



This process creates a bit file that is used to program the Spartan-3E chip. Again, after this process is finished, green check marks should be shown.

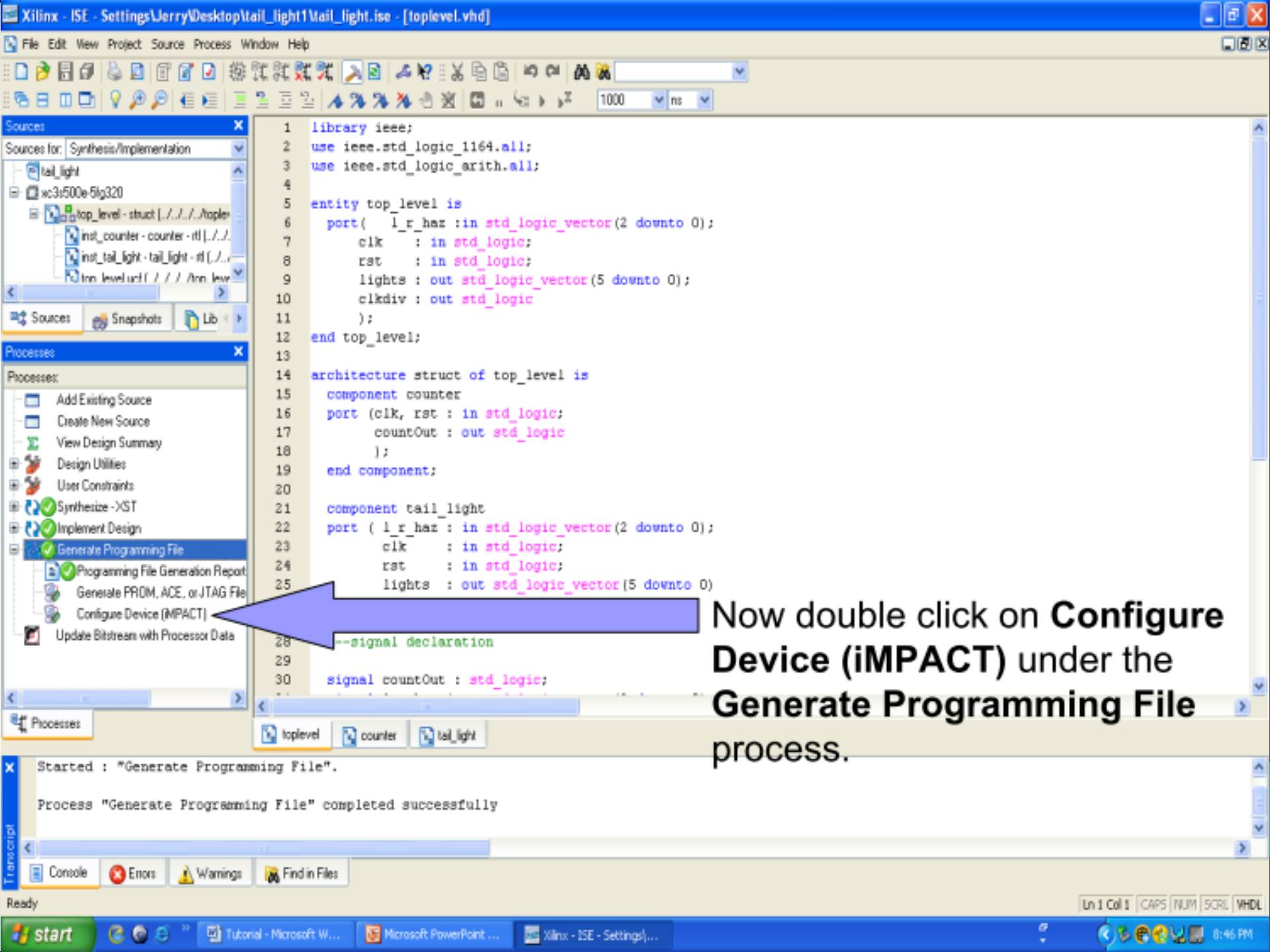
FPGA

- Now you are ready to program the Spartan-3E chip. Plug-in the USB cable to the computer. Connect the FPGA Spartan-3E board to power **FIRST**, then connect the USB cable to the board. This order must be followed for the Spartan-3E chip to be programmed properly.

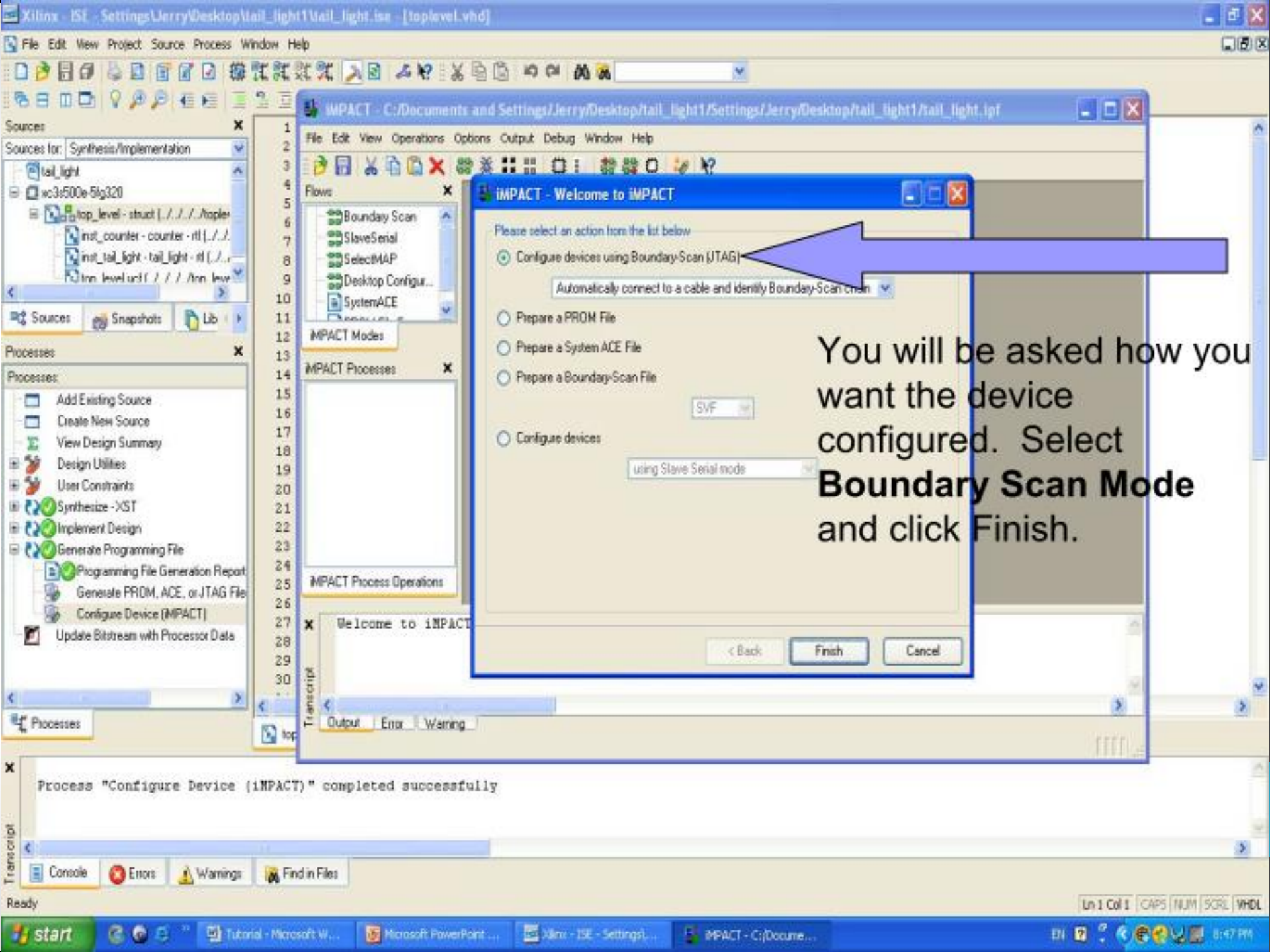

POWER is ON
Micron
LINEAR
TEXAS INSTRUMENTS
Platform Flash
XILINX
DIGILENT®
www.digilentinc.com
SPARTAN-3E
FPGA
smsc
Intel
Flash
Memory

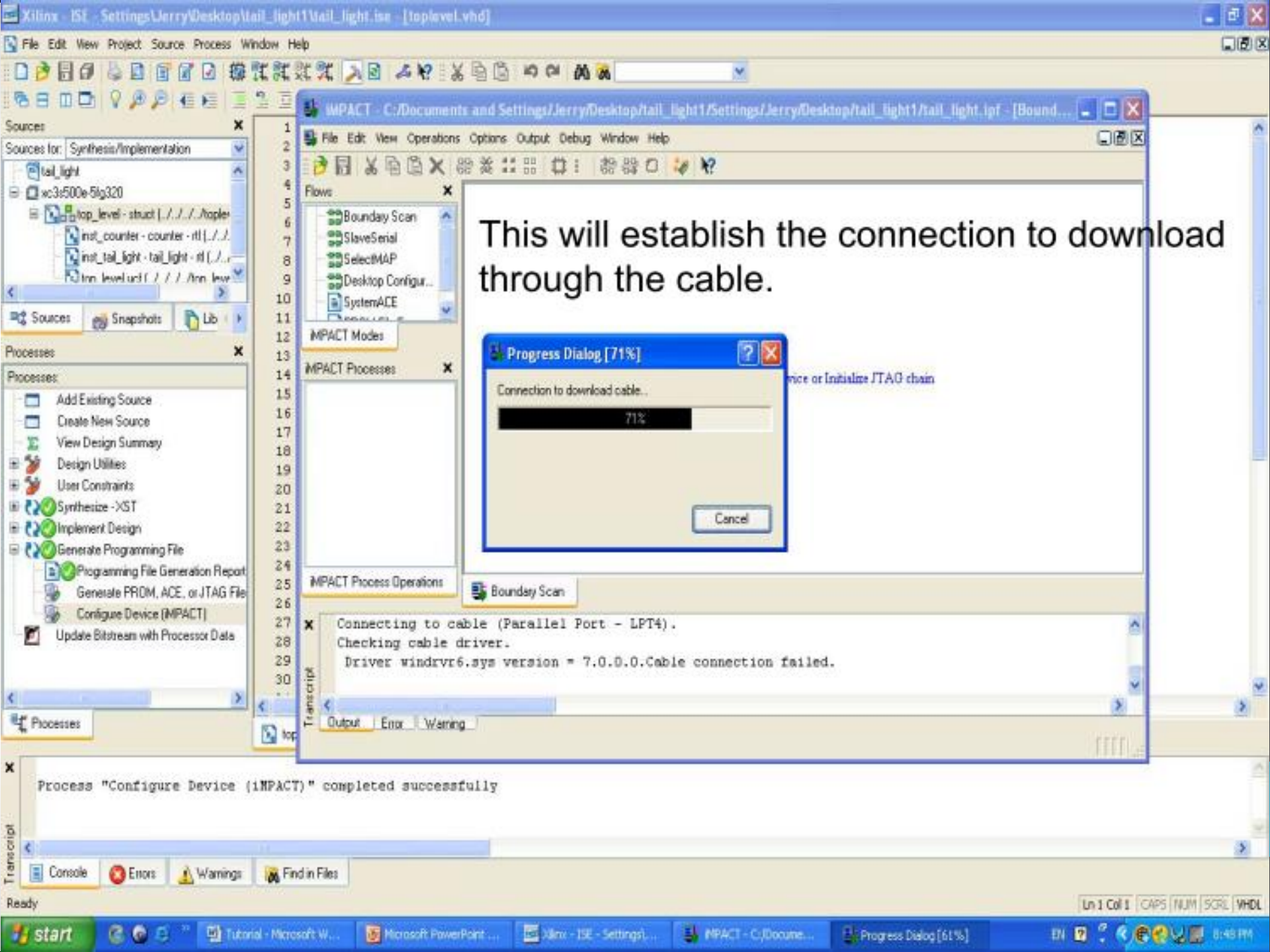

HIGH SPEED
HALO
GND
VCC
C185
IC6
J19
C51
X1
IC4
J8
BTN West
NC Connector

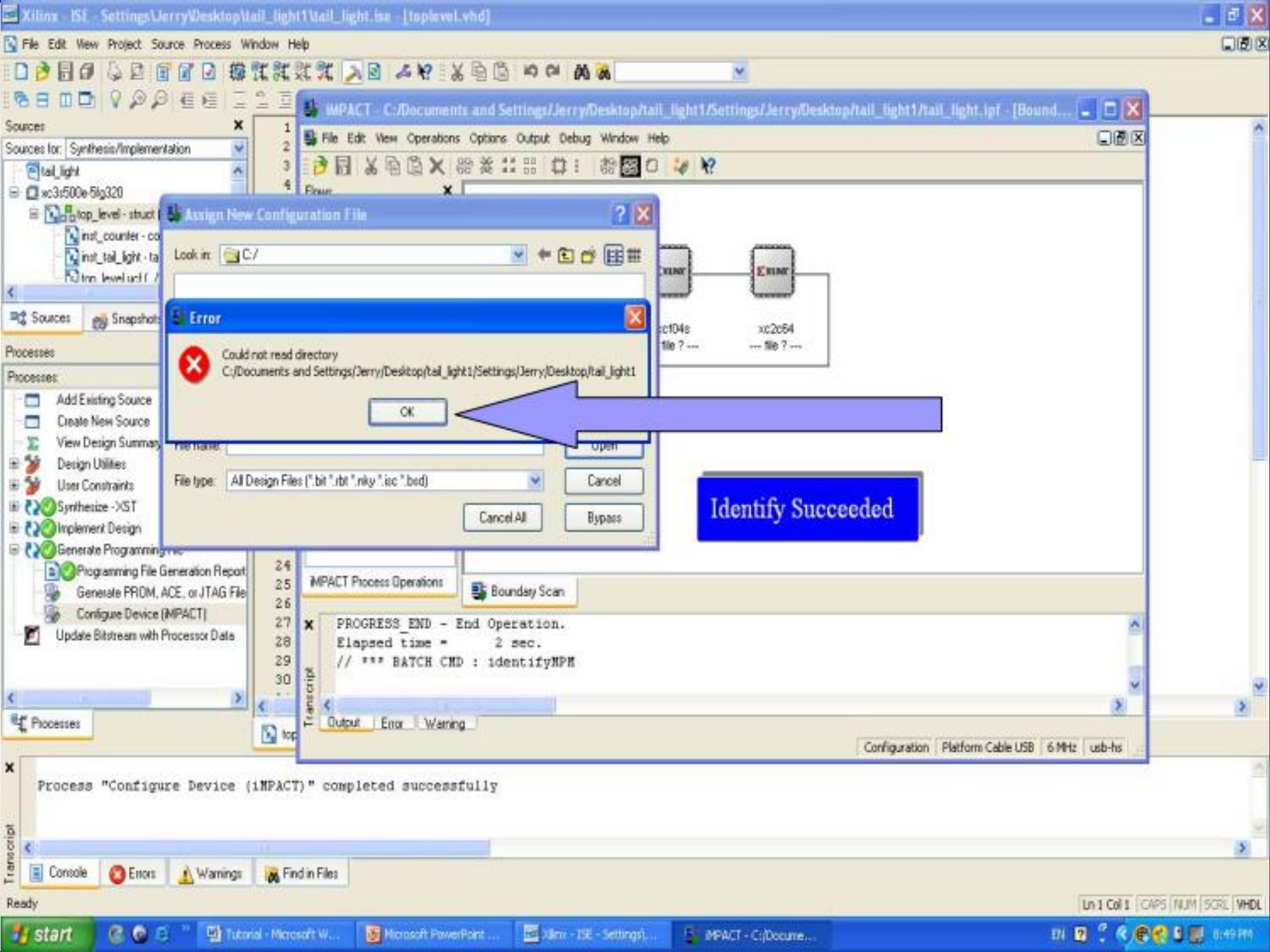

TEXAS INSTRUMENTS
DIGILENT®
www.digilentinc.com
smsc
The system will automatically install the driver. If the driver is installed correctly, the green light should be displayed

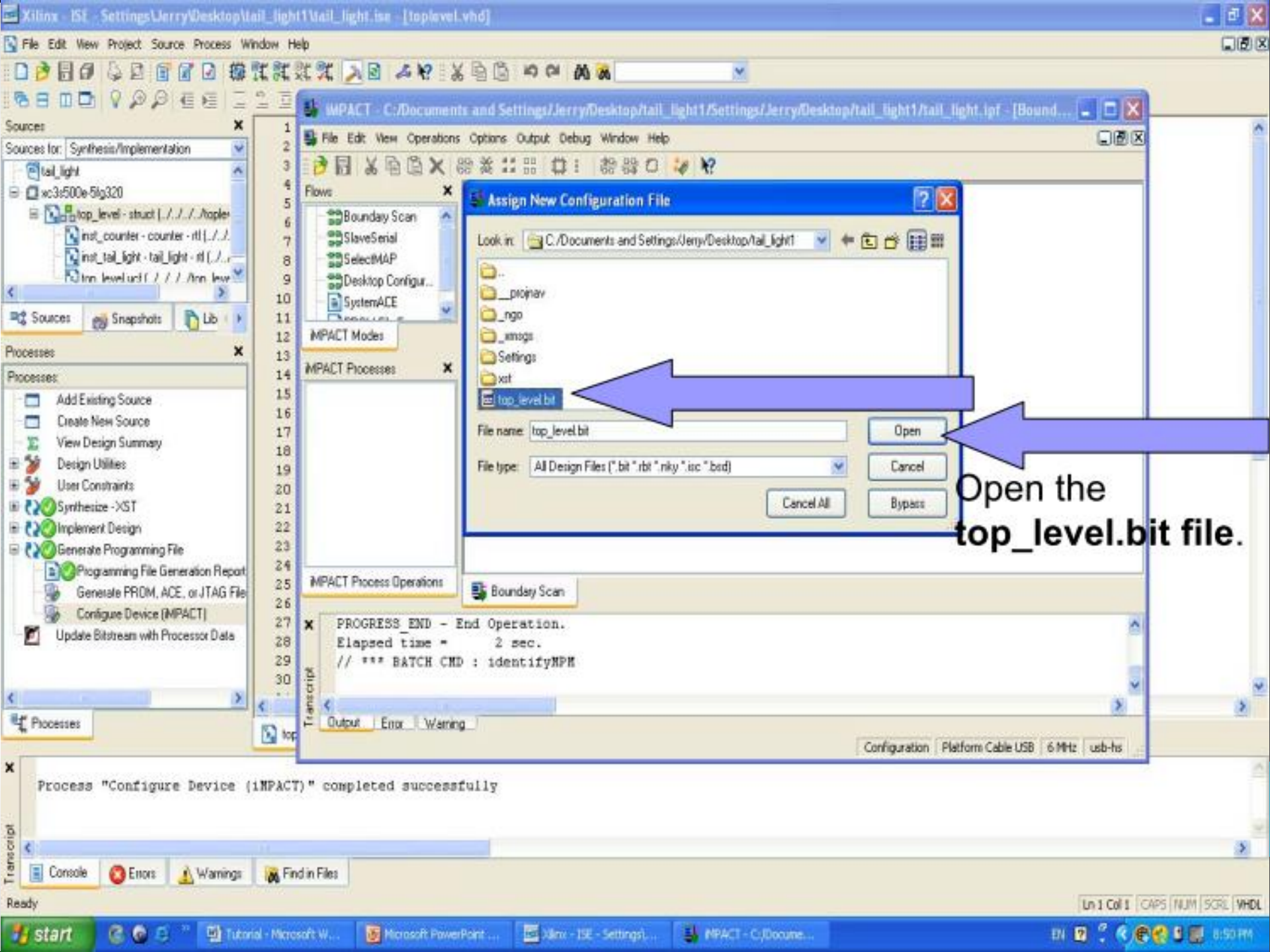


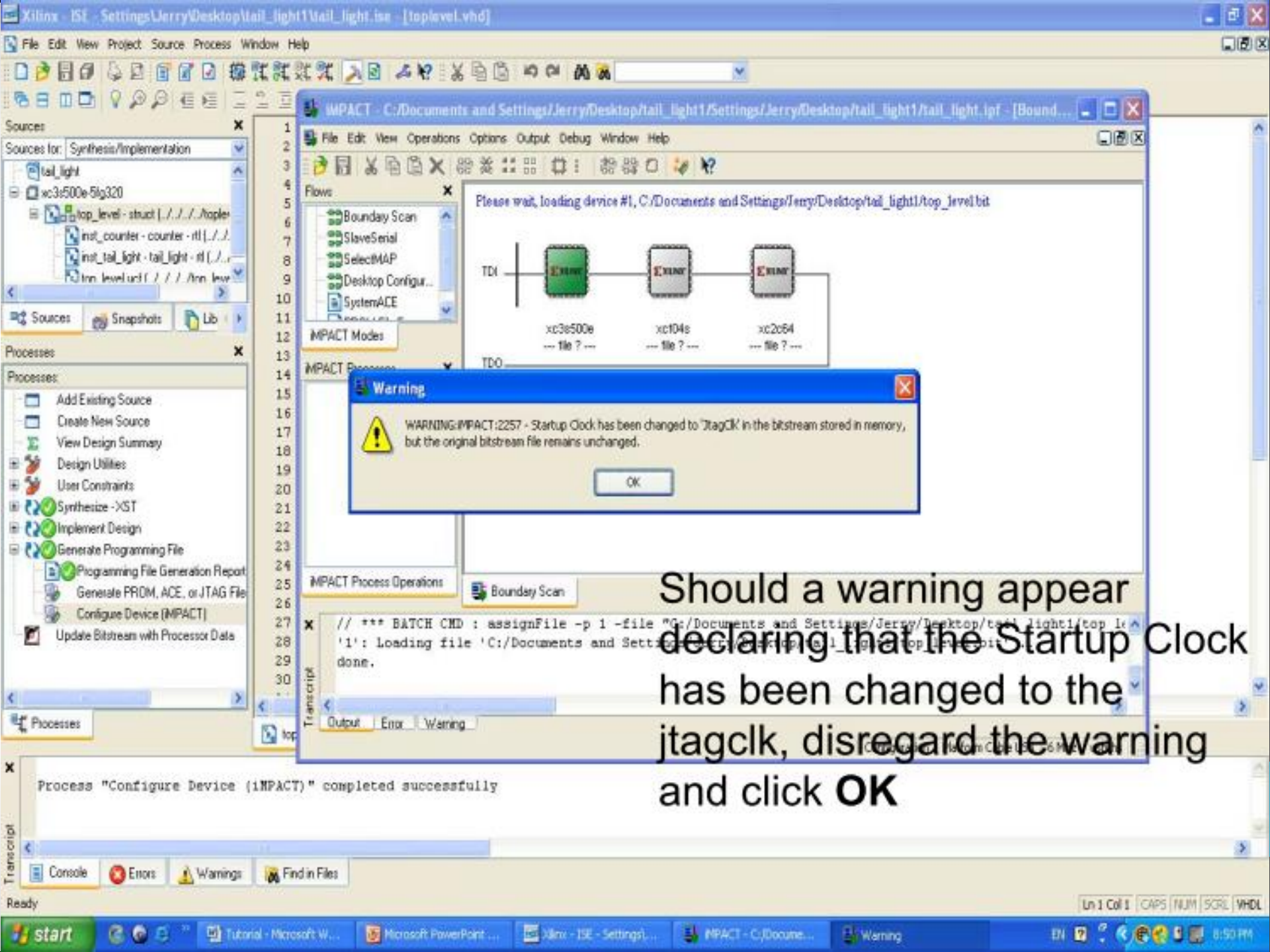
Now double click on **Configure Device (iMPACT)** under the **Generate Programming File** process.

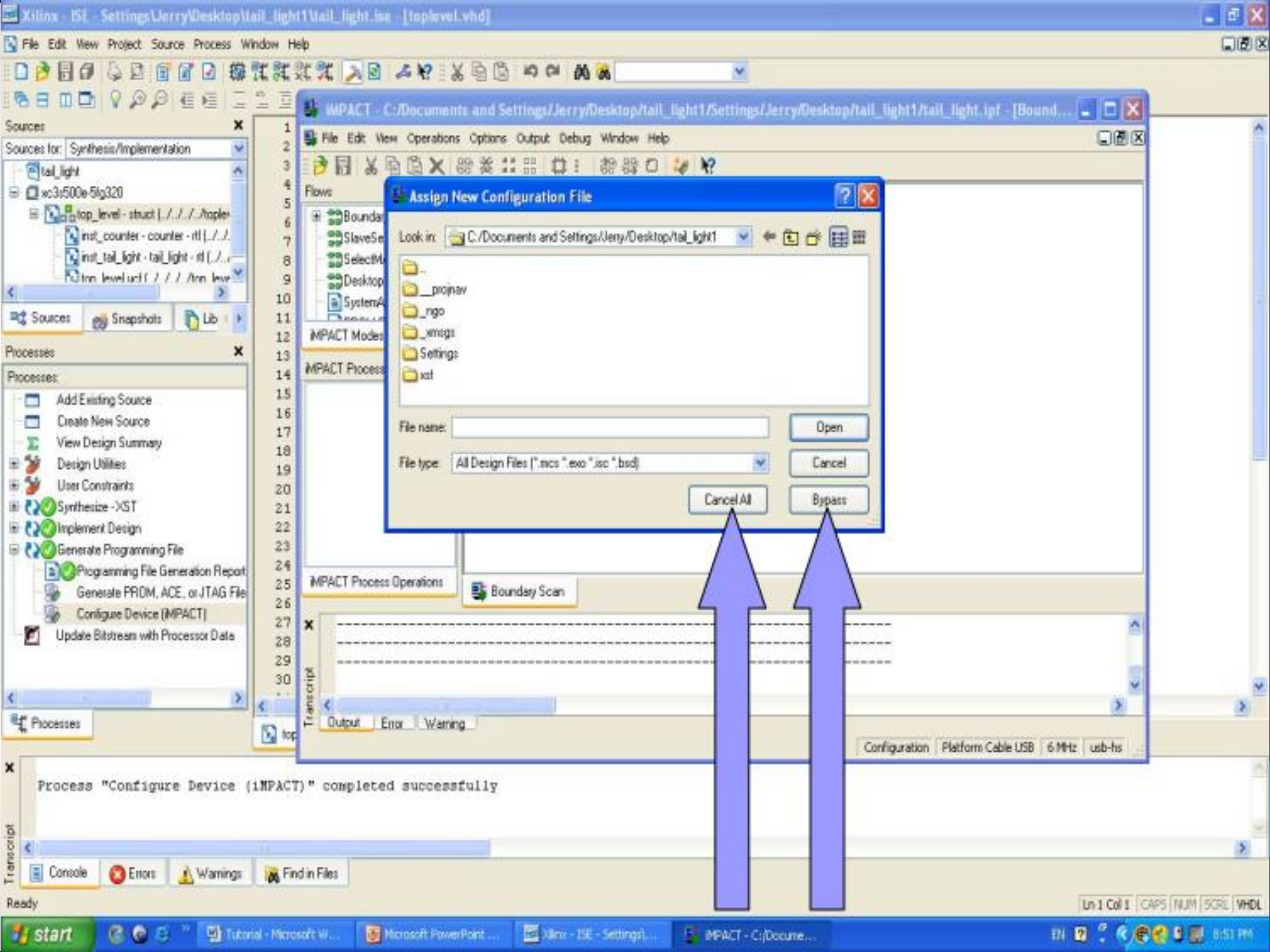

iMPACT - Welcome to iMPACT
Please select an action from the list below
Configure devices using Boundary-Scan (JTAG)
Automatically connect to a cable and identify Boundary-Scan chain
Prepare a PROM File
Prepare a System ACE File
Prepare a Boundary-Scan File
SVF
Configure devices
using Slave Serial mode
< Back
Finish
Cancel
You will be asked how you want the device configured. Select **Boundary Scan Mode** and click Finish.
Process "Configure Device (iMPACT)" completed successfully

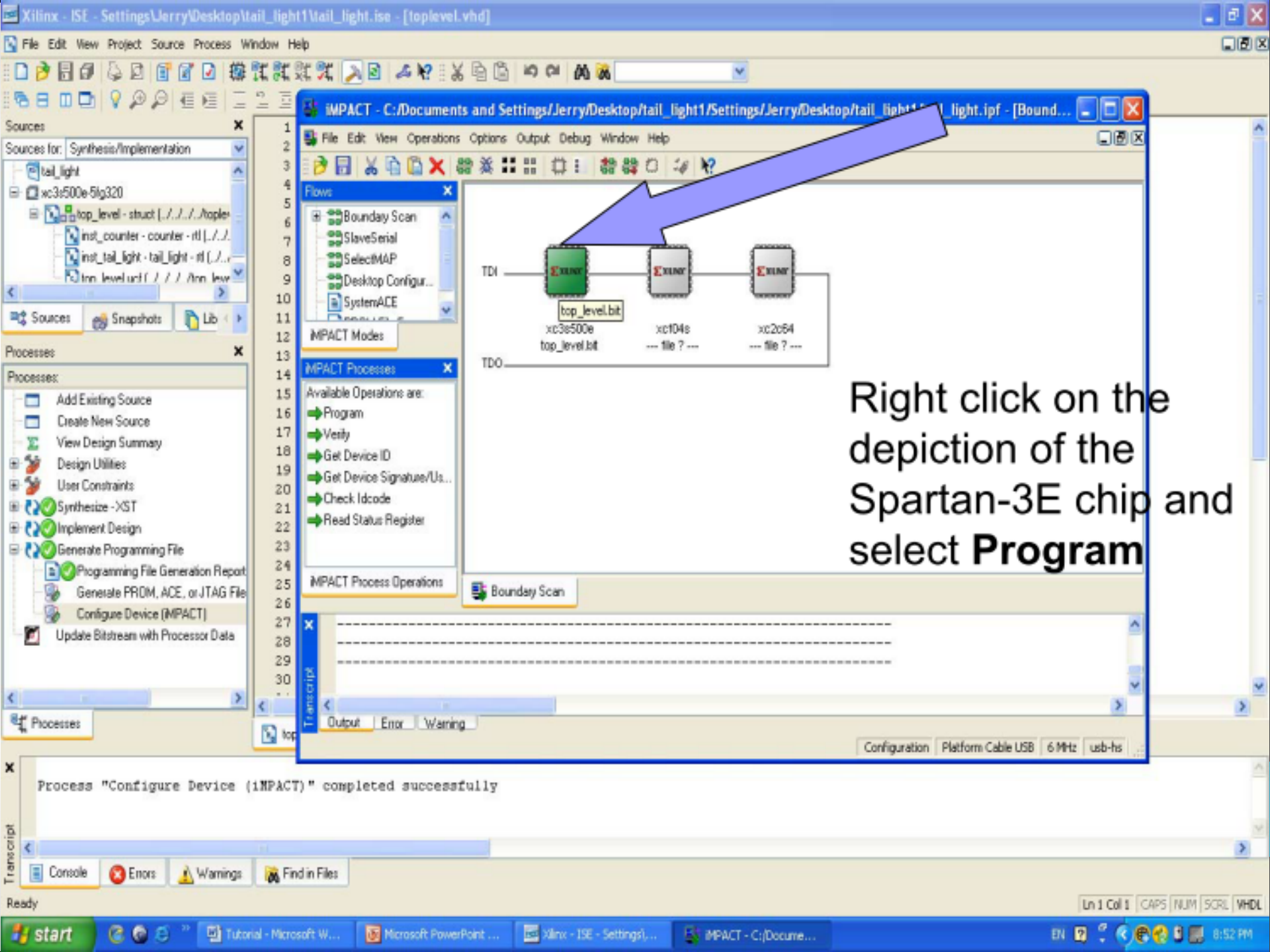

This will establish the connection to download through the cable.
Progress Dialog [71%]
Connection to download cable...
71%
Cancel
Connecting to cable (Parallel Port - LPT4).
Checking cable driver.
Driver windrvr6.sys version = 7.0.0.0.Cable connection failed.
Process "Configure Device (iMPACT)" completed successfully
Ready

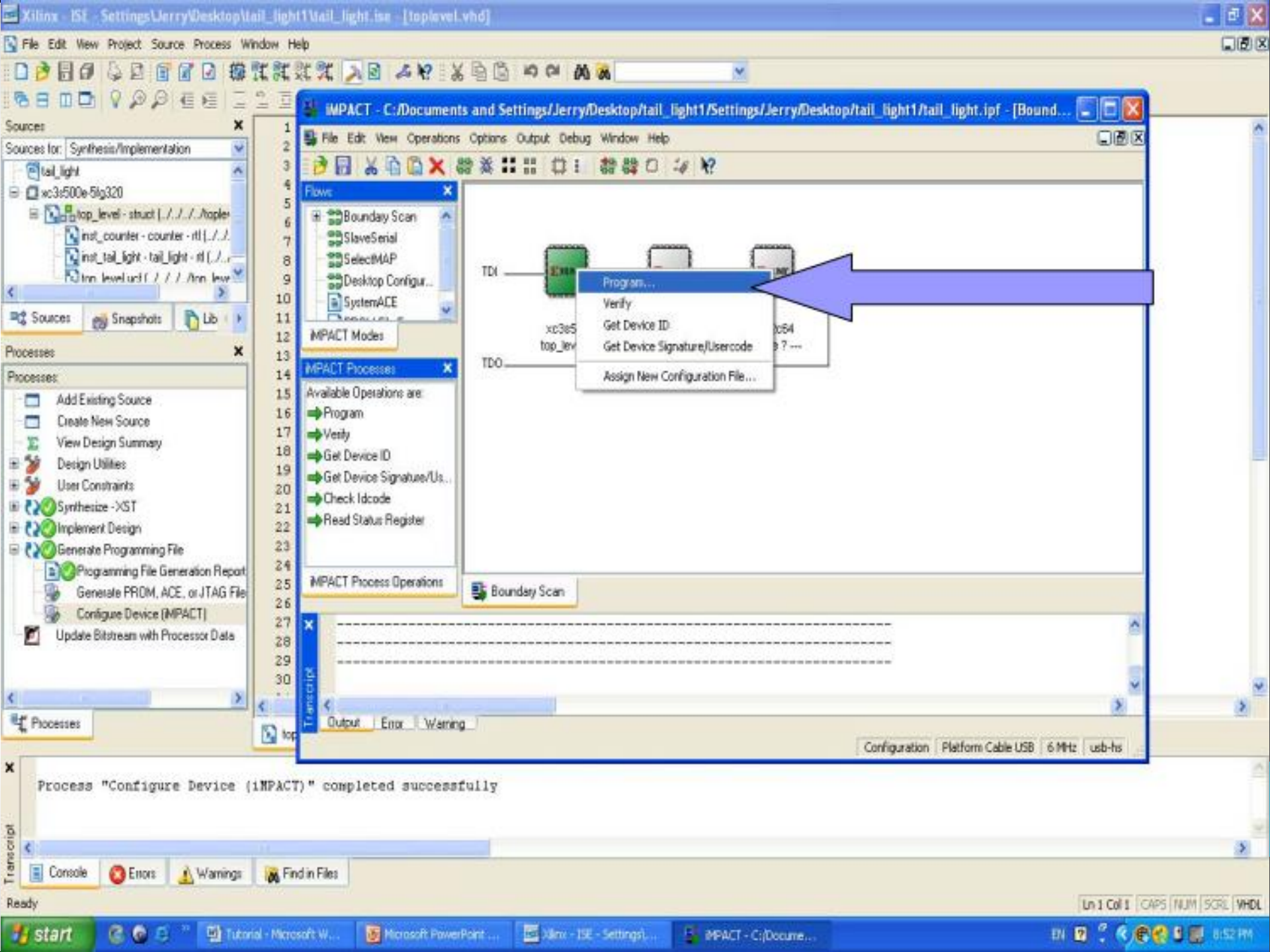

Assign New Configuration File
Look in: C:/
Error
Could not read directory
C:/Documents and Settings/Jerry/Desktop/tail_light1/Settings/Jerry/Desktop/tail_light1
OK
File type: All Design Files (*.bit *.rbt *.nky *.isc *.bsd)
Open
Cancel
Cancel All
Bypass
Identify Succeeded
PROGRESS_END - End Operation.
Elapsed time = 2 sec.
// *** BATCH CMD : identifyMPM
Process "Configure Device (iMPACT)" completed successfully

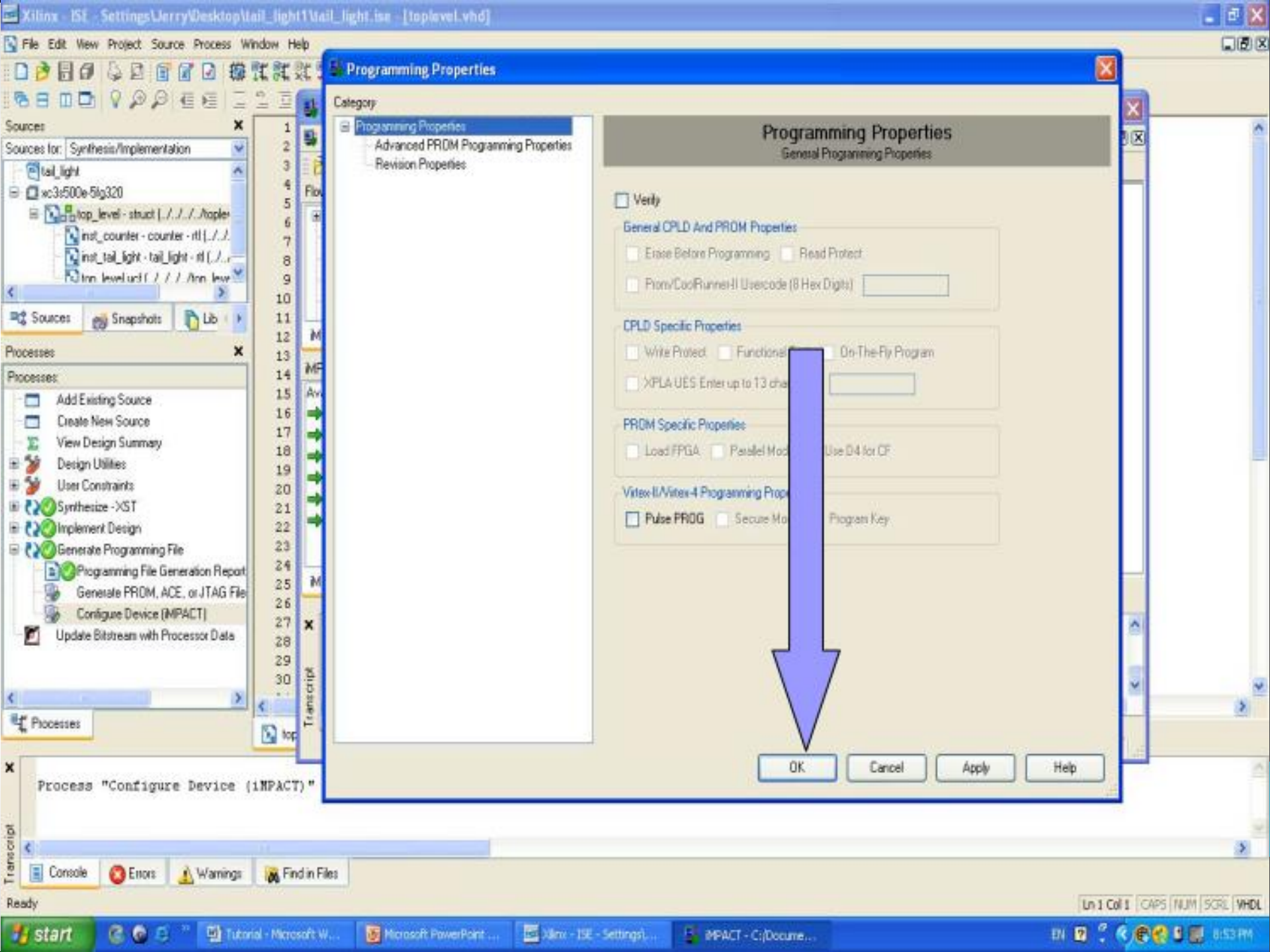

Assign New Configuration File
Look in: C:/Documents and Settings/Jerry/Desktop/tail_light1
top_level.bit
File name: top_level.bit
File type: All Design Files (*.bit *.rbt *.nky *.isc *.bsd)
Open
Cancel
Cancel All
Bypass
Open the top_level.bit file.
PROGRESS_END - End Operation.
Elapsed time = 2 sec.
// *** BATCH CMD : identifyMPM
Process "Configure Device (iMPACT)" completed successfully

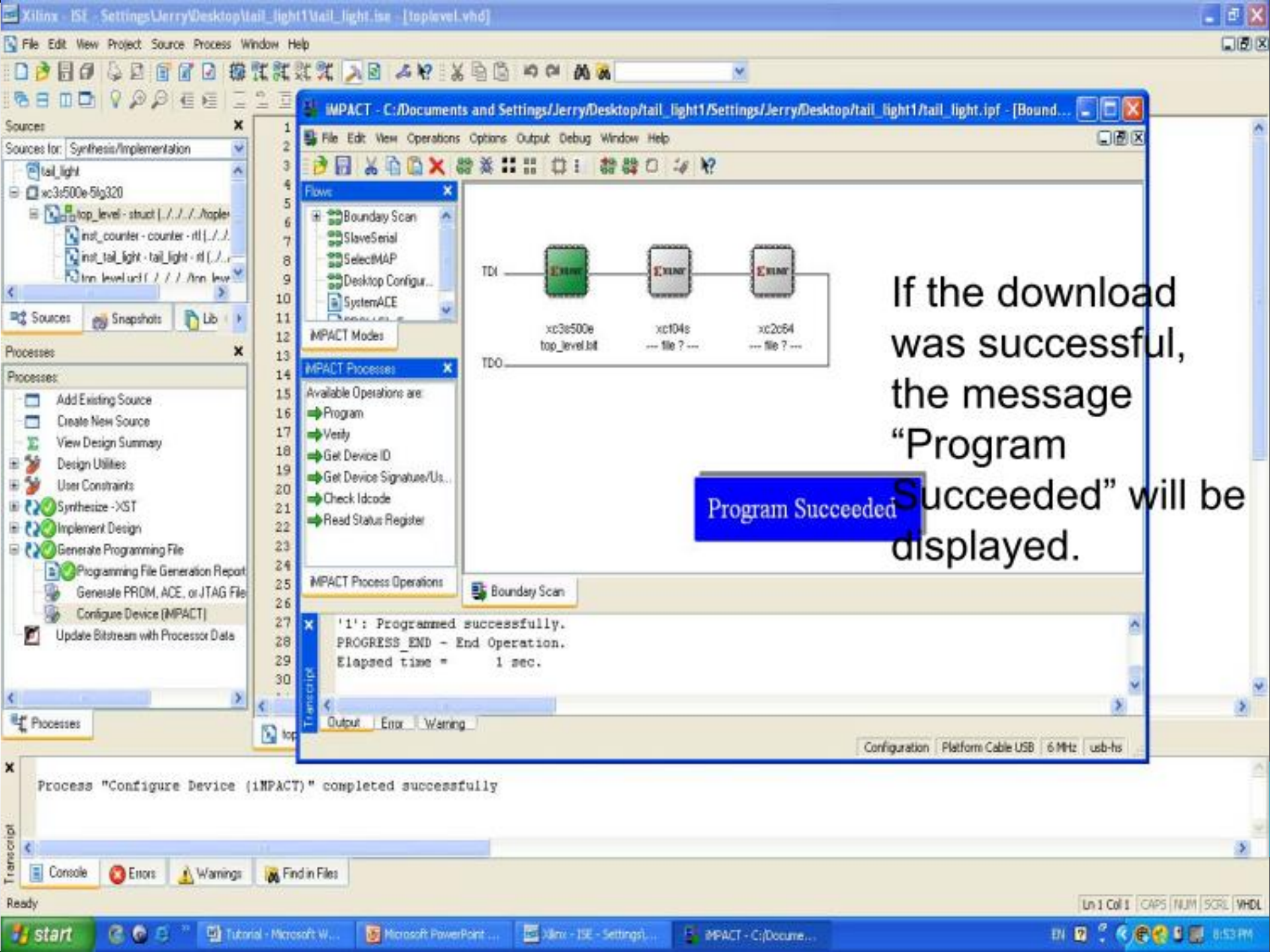

Warning
WARNING:iMPACT:2257 - Startup Clock has been changed to 'JtagClk' in the bitstream stored in memory, but the original bitstream file remains unchanged.
OK
Please wait, loading device #1, C:/Documents and Settings/Jerry/Desktop/tail_light1/top_level.bit
TDI
TDO
xc3s500e
xc104s
xc2c64
Should a warning appear declaring that the Startup Clock has been changed to the jtagclk, disregard the warning and click **OK**


Assign New Configuration File
Look in: C:/Documents and Settings/Jerry/Desktop/tail_light1
__projnav
_ngo
_xmsgs
Settings
xst
File name:
File type: All Design Files (*.mcs *.exo *.isc *.bsd)
Open
Cancel
Cancel All
Bypass
Process "Configure Device (iMPACT)" completed successfully


Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise - [toplevel.vhd]
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementation
tail_light
xc3s500e-5fg320
top_level - struct (../../../../toplev
inst_counter - counter - rtl (../../
inst_tail_light - tail_light - rtl (../..
Sources
Snapshots
Processes
Processes:
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Programming File Generation Report
Generate PROM, ACE, or JTAG File
Configure Device (iMPACT)
Update Bitstream with Processor Data
Processes
iMPACT - C:/Documents and Settings/Jerry/Desktop/tail_light1/Settings/Jerry/Desktop/tail_light1/tail_light.ipf - [Bound...
File Edit View Operations Options Output Debug Window Help
Flows
Boundary Scan
SlaveSerial
SelectMAP
Desktop Configur...
SystemACE
iMPACT Modes
iMPACT Processes
Available Operations are:
Program
Verify
Get Device ID
Get Device Signature/Us...
Check Idcode
Read Status Register
iMPACT Process Operations
TDI
TDO
top_level.bit
xc3s500e
top_level.bit
xc104s
--- file ? ---
xc2c64
--- file ? ---
Boundary Scan
Right click on the depiction of the Spartan-3E chip and select Program
Transcript
Output
Error
Warning
Configuration
Platform Cable USB
6 MHz
usb-hs
Process "Configure Device (iMPACT)" completed successfully
Console
Errors
Warnings
Find in Files
Ready
Ln 1 Col 1
CAPS
NUM
SCRL
VHDL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
iMPACT - C:\Docume...
EN
8:52 PM


Xilinx - ISE - Settings\Jerry\Desktop\tail_light1\tail_light.ise - [toplevel.vhd]
File Edit View Project Source Process Window Help
Sources
Sources for: Synthesis/Implementation
tail_light
xc3s500e-5fg320
top_level - struct [../../../../toplev
inst_counter - counter - rtl [../../
inst_tail_light - tail_light - rtl [../..
Sources
Snapshots
Lib
Processes
Processes:
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Programming File Generation Report
Generate PROM, ACE, or JTAG File
Configure Device (iMPACT)
Update Bitstream with Processor Data
Processes
iMPACT - C:/Documents and Settings/Jerry/Desktop/tail_light1/Settings/Jerry/Desktop/tail_light1/tail_light.ipf - [Bound...
File Edit View Operations Options Output Debug Window Help
Flows
Boundary Scan
SlaveSerial
SelectMAP
Desktop Configur...
SystemACE
iMPACT Modes
iMPACT Processes
Available Operations are:
Program
Verify
Get Device ID
Get Device Signature/Us...
Check Idcode
Read Status Register
iMPACT Process Operations
TDI
TDO
Program...
Verify
Get Device ID
Get Device Signature/Usercode
Assign New Configuration File...
Boundary Scan
Transcript
Output
Error
Warning
Configuration
Platform Cable USB
6 MHz
usb-hs
Process "Configure Device (iMPACT)" completed successfully
Console
Errors
Warnings
Find in Files
Ready
Ln 1 Col 1
CAPS
NUM
SCRL
VHDL
start
Tutorial - Microsoft W...
Microsoft PowerPoint ...
Xilinx - ISE - Settings\...
iMPACT - C:\Docume...
EN
8:52 PM


Programming Properties
Category
Programming Properties
Advanced PROM Programming Properties
Revision Properties
Programming Properties
General Programming Properties
Verify
General CPLD And PROM Properties
Erase Before Programming
Read Protect
Prom/CoolRunner-II Usercode (8 Hex Digits)
CPLD Specific Properties
Write Protect
On-The-Fly Program
PROM Specific Properties
Load FPGA
Use D4 for CF
Virtex-II/Virtex-4 Programming Prop
Pulse PROG
Program Key
OK
Cancel
Apply
Help
Sources
Sources for: Synthesis/Implementation
tail_light
xc3s500e-5fg320
Processes
Add Existing Source
Create New Source
View Design Summary
Design Utilities
User Constraints
Synthesize - XST
Implement Design
Generate Programming File
Programming File Generation Report
Generate PROM, ACE, or JTAG File
Configure Device (iMPACT)
Update Bitstream with Processor Data
Process "Configure Device (iMPACT)"
Console
Errors
Warnings
Find in Files
Transcript
Ready
Ln 1 Col 1
CAPS
NUM
SCRL
VHDL
start


iMPACT - C:/Documents and Settings/Jerry/Desktop/tail_light1/Settings/Jerry/Desktop/tail_light1/tail_light.ipf - [Bound...
TDI
TDO
xc3s500e
top_level.bit
xc104s
--- file ? ---
xc2c64
--- file ? ---
Program Succeeded
If the download was successful, the message "Program Succeeded" will be displayed.
'1': Programmed successfully.
PROGRESS_END - End Operation.
Elapsed time = 1 sec.
Process "Configure Device (iMPACT)" completed successfully


Intel
Flash
Memory
FPGA
PB200-087
REV B1
J31
J4
J1
J2
J3
GND
VCC
SMA-CLK(A10)

FPGA Demo


Intel
Flash
Memory
FPGA
PB200-087
REV B1
J31
J4
J1
J2
J3
GND
VCC
SMA-CLK(A10)

- For more details, refer to:
  - **Computer Aided Design of Electronics** *course lecture notes*.
  - **The VHDL Cookbook**, *Peter J. Ashenden, 1st edition, 1990.*
- The lecture is available online at:
  - http://bu.edu.eg/staff/ahmad.elbanna-courses/12135
- For inquires, send to:
  - ahmad.elbanna@feng.bu.edu.eg